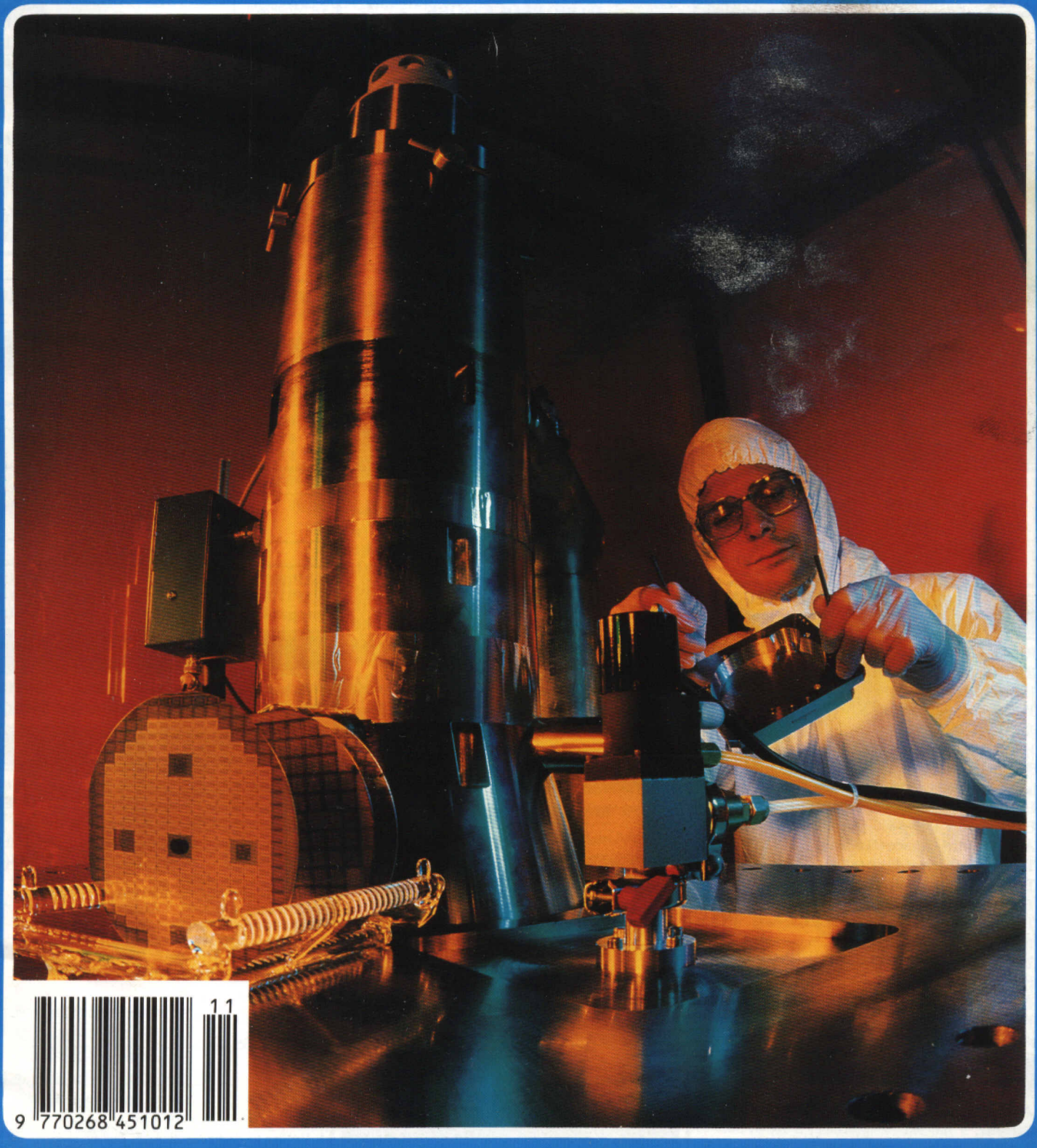
THE ELECTRONICS MAGAZINE WITH THE PRACTICAL APPROACH
UK £1·70 IR £2·62 (incl. VAT) November 1989

Elektor Electronics

Extension card for Archimedes
CMOS preamplifier
EPROM simulator
8098 evaluation board
Speeding up the computer
3½ LED-digit SMD voltmeter
Computer mouse
Multiplex control with U6050/6052



9 770268 451012 11

Elektor Electronics

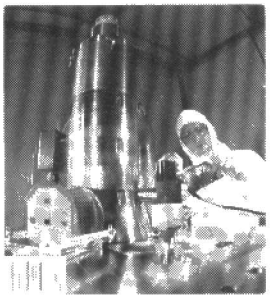
November 1989
Volume 15
Number 172

CONTENTS

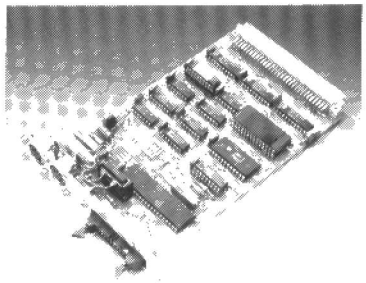
Theme of the month in December will be Test & Measurement.

Also in the December issue:
- Digital signal processing
- CMOS preamplifier*
- EPROM simulator*
- Hard disk monitor
- Transistor curve tracer
- AF/HF signal tracer
- The digital model train (9)

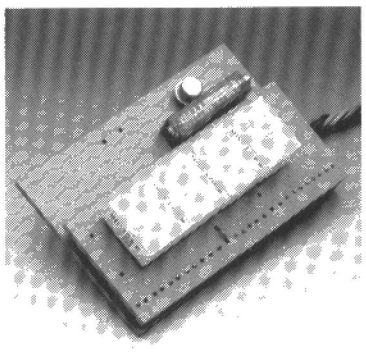
* We regret that owing to circumstances beyond our control neither CMOS preamplifier nor EPROM simulator could be published in the current issue.



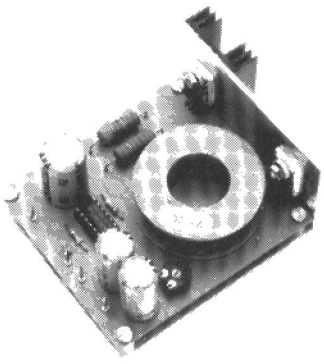
Front cover
In the design of a new or improved electronics product, new ICs are often the key to success. Unfortunately, even large electronics companies rarely have the in-house expertise to design ICs to new and exact requirements. Often, therefore, the design is a compromise, which is safer and less time consuming. Qudos of Cambridge have developed a system to overcome this problem. The system uses the latest electron beam technology, which enables direct write-on-silicon to allow up to 250 different designs to be transcribed on to a single wafer. With an industry standard of six to eight weeks, transcription can now be completed in one.



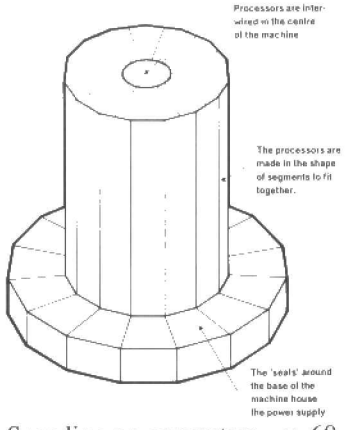
Extension card for Archimedes
p. 12



3.5-digit SMD voltmeter – p. 37



DC-DC power converter – p. 54



Speeding up computers – p. 60

ELEKTOR ELECTRONICS (Publishing)
Editor/publisher: Len Seymour
Technical Editor: J Buiting

Editorial offices:
Down House
Broomhill Road
LONDON SW18 4JQ
England
Telephone: 01-877 1688 *(National)*
or +44 1877 1688 *(International)*
Telex: 917003 (LPC G)
Fax: 01-874 9153 *(National)*
+44 1874 9153 *(International)*

Advertising: PRB Ltd
3 Wolseley Terrace
CHELTENHAM GL50 1TH
Telephone: (0242) 510760
Fax: (0242) 226626

European offices:
Postbus 75
6190 AB BEEK (L)
The Netherlands
Telephone: +31 4490 89444
Telex: 56617 (elekt nl)
Fax: +31 4490 70161

Managing Director: M.M.J. Landman

Overseas editions:

Federal Germany
Elektor Verlag GmbH
Süsterfeld-Straße 25
5100 Aachen
Editor: E J A Krempelsauer

France
Elektor sarl
Route Nationale; Le Seau; B.P. 53
59270 Bailleul
Editors: D R S Meyer;
G C P Raedersdorf

Greece
Elektor EPE
Karaiskaki 14
16673 Voula – Athens
Editor: E Xanthoulis

India
Elektor Electronics PVT Ltd.
Chhotani Building
52 C, Proctor Road, Grant Road (E)
Bombay 400 007
Editor: Surendra Iyer

Netherlands
Elektuur B.V.
Peter Treckpoelstraat 2-4
6191 VK Beek
Editor: P E L Kersemakers

Pakistan
Electro-shop
35 Naseem Plaza
Lasbella Chawk
Karachi 5
Editor: Zain Ahmed

Portugal
Ferreira & Bento Lda.
R.D. Estefânia, 32-1°
1000 Lisboa
Editor: Jeremias Sequeira

Spain
Ingelek S.A.
Plaza República Ecuador
2-28016 Madrid

Sweden
Electronic Press AB
Box 5505
14105 Huddinge
Editor: Bill Cedrum

Distribution:
SEYMOUR
1270 London Road
LONDON SW16 4DH.

Written and composed on Apple and IBM corporate publishing systems by Elektor Electronics.

Printed in the Netherlands by NDB, Zoeterwoude.

UK TV STEREO SYSTEM

Test transmissions have started in London and parts of northern England with a new British television sound system that has been recommended by the European Broadcasting Union (EBU). A preliminary service with it will follow in the same areas within a few months. It is planned to be available to 75% of the British population by the end of next year.

Stereo sound has already been introduced in some countries, but the lack of international standardization has resulted in a proliferation of systems for adding the additional stereo information at the transmitter and decoding it in the receiver.

It was the shortcomings of these stereo systems, as used, for instance, in Federal Germany and the USA, that encouraged the BBC to develop a technically superior digital system, known as NICAM 728, for use in the UK. The Independent Broadcasting Authority (IBA) co-operated in the later stages of its development and the production of an agreed specification with the receiver industry. NICAM 728 has been adopted by a number of other countries in preference to the German or American systems and is now the digital system recommended by the EBU.

The main features of NICAM 728 are its compatibility with existing receivers, quality and ruggedness. The digitized stereo sound is transmitted separately from the normal sound, which ensures freedom of perceptible interference on existing receivers. Another feature is the total separation between the left and right channels, which enables them to be used independently, for instance, to broadcast in separate languages. For that reason, the term Dual Channel Sound—DCS—is normally used to describe the new service.

Audio quality approaching that of the compact disc is assured by the digital techniques used in the new system. Error detection is used to enable the receiver to provide an error-free output even under adverse reception conditions where the signal may be fading or be subject to reflections from tall buildings.

At present, vision and sound signals are distributed over separate circuits, mainly provided by British Telecom. Although it would have been possible to rent new circuits for DCS, this would have been an expensive option. Instead, a technique known as 'sound–in–syncs' (SIS) is to be used.

With SIS, the left and right sound signals are digitally coded into a data stream, which is then carried within the vision synchronizing pulses. Thus, the sound signal is, in effect, 'piggy-backed' on the vision signal, enabling engineers to dispense with separate sound circuits.

MORE POWER AND CAPACITY FOR NEW INMARSAT SATELLITES

The new generation of communication satellites planned by the International Maritime Satellite Organization (INMARSAT) for the 1990s and beyond will have 30 times the capacity of its present satellites.

INMARSAT says the new network will be highly flexible and capable of dynamically reallocating power and bandwidth on a global scale. This will allow the organization to provide special coverage facilities to cope with particular service needs or emergencies around the world. The total effective isotropically radiated power (EIRP) of the satellites will be 48 dBW, nearly 10 times that of INMARSAT II satellites due to be launched over the next two years or 30 times the capacity of the satellites currently in operation.

The liftoff mass is expected to be of the order of 1800–2500 kg and the satellites will have a minimum of four spot beams for mobile communications in important service areas in addition to global coverage. Other features that may be incorporated are L-to-L band connections that will allow direct mobile-to-mobile communications, and C-to-C band connections for system administration between coast earth stations.

SCOTTISH DESIGN SUCCESS FOR NEW MICROCOMPUTER

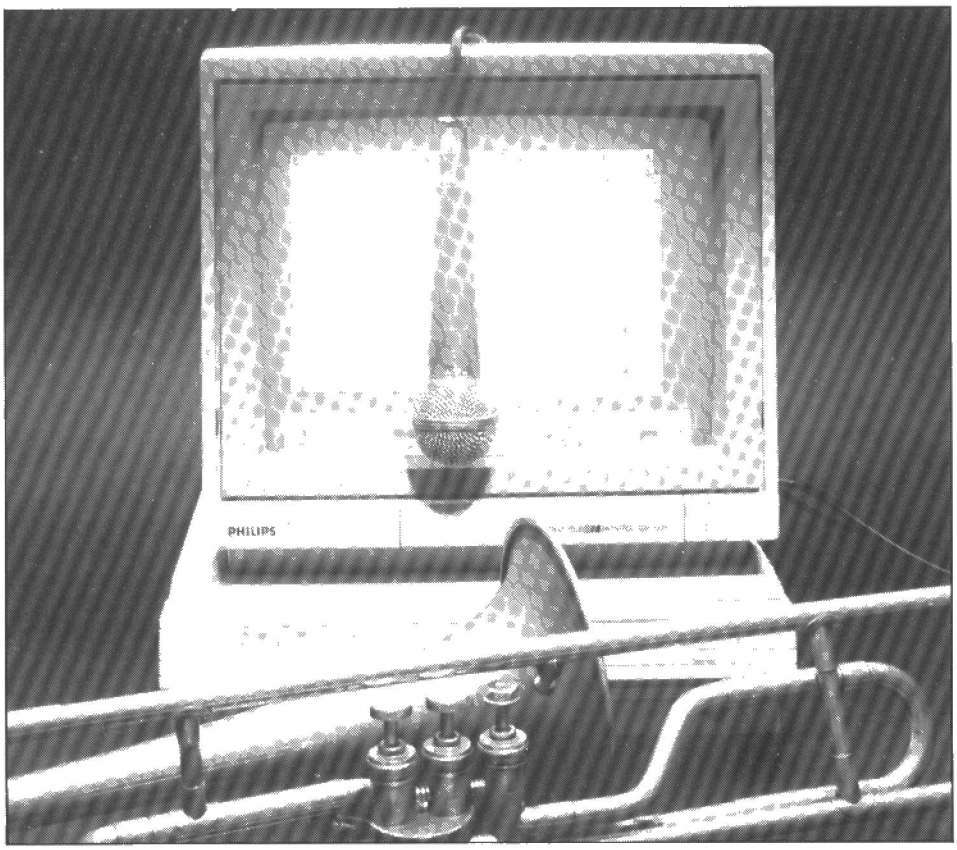
Engineers at Digital Equipment's Scottish plant have recently completed design work on a new high-powered microcomputer six months ahead of schedule and at two-thirds of the originally estimated cost of £3 million.

The Type 3100, the first high-powered microcomputer to be designed and built totally in Scotland, has twice the memory capacity, three times the CPU power and five times the storage capacity of its predecessor MicroVax 2000. It is suitable for use in engineering, marketing, finance, office information systems, and small businesses with word processing, accounting, payroll, personnel and inventory control.

EXTENSION CARD FOR ARCHIMEDES

The Acorn Archimedes is a Reduced Instruction Set Computer (RISC) that handles complex graphics, number crunching, music applications and I/O activities at a speed that makes owners of 286-based and many other PCs sit back in awe. The extension card described in this article gives the 'Archie' yet more power and versatility by adding a MIDI interface, a sound sampler and a user port.

W. van Dalen



Acorn Computers (a member of the Olivetti Group) have always been known for their rather uncommon approach of computer design. Their advanced systems are invariably relatively fast, flexible, and innovative. The system architecture is so open as to allow many electronics and computer enthusiasts to embark on home construction of extension cards. From a point of view of computer education, Acorn have been backed successfully by the BBC with the well-known BBC-B and Master computers, the predecessors of the Archimedes.

The introduction of the Archimedes A3000 roughly a year ago allowed many computer enthusiasts to partake, at reasonable cost, in the excitement of true 32-bit RISC programming. No doubt the A3000 will claim its very own place in the modern computing scene as one of the fastest and most versatile PCs.

The Archimedes extension card offers a MIDI interface for computer music applications, a sound sampler with control software, and an 8-bit I/O port that allows many peripherals originally designed for the BBC-B computer, such as the renowned BBC Buggy, to be controlled by the Archimedes.

System architecture

Before discussing the operation of the extension card, it is useful to look at the system architecture of the Archimedes. Extension cards for the Archimedes are called podules, and every Archimedes computer has room for 4 of these. The computers in the 3000 series, however, require a backplane before the podules can be installed. This backplane connects the motherboard to the podule(s). Acorn supplies a double backplane, but most versions found on the market are quadruple types. The present podule can be installed on a double as well as a quadruple backplane. A small fan is, however, required in both cases.

The hardware core of the Archimedes is formed by 4 chips: the CPU, better known as the ARM (Acorn RISC module), the MEMC (memory controller), the IOC (I/O controller) and the VIDC (video controller).

The memory is divided into blocks of 4, 8, 16 or 32 KByte. The size of the blocks depends on the maximum amount of memory fitted. In a 512 kByte machine, the blocks are 4 KByte each, in a 1 MByte machine 8 KByte, in a 2 MB machine 16 KByte, and, finally, in a 4 MB machine they are 32 KByte each. Currently, the maximum memory size for the Archimedes 3000 is 4 MByte.

The MEMC assigns a logic memory location to a physical memory block. This dynamic division ensures the best possible use of available memory at all times. The video interface, for instance, is assigned just the amount of memory it requires for the selected mode. The same applies to the sound channel or to any other buffer.

The I/O channels are also controlled in

a fairly tightly regulated configuration, the hardware consequences of which for the present podule will be reverted to.

Most software used to enable the Archimedes to control peripheral equipment is written in the form of modules. Each module is a piece of relocatable software that is automatically recognized by the computer's internal control system. The user may call these routines direct.

The present podule is no different from commercially available types for other applications in that it accepts a ROM with control software. The computer, on finding a podule with a ROM, automatically loads the software module and makes the commands offered by it available to the user. The module and its commands are gone the moment the podule is removed from the computer. The sound sampler on the present podule can use the ROM sold by Acorn as the MIDI upgrade for their I/O podule. This ROM contains the commands for the user port and the I/O port. The sound sampler itself does not use the ROM-based commands, but separate software, supplied on a 3½-inch disk through the Readers Services under order number ESS 105.

Extension card and the motherboard

The backplane has 2 or 4 connectors that accept a podule. In principle, the backplane is suitable for 4 different podules. The one described here is actually composed of two podules: a memory podule and a simple podule. Each of these has its own selection signal: $\overline{MS}$ for the memory podule, and $\overline{PS}$ for the simple podule.

The pinning of the backplane connector is shown in Fig. 1. It should be noted that only the A and C rows are used — the B row is reserved for co-processors, and is available only on podule slot 2 of Archimedes computers in the 400 series. The present podule communicates with the computer via the 64-way connector, and can be installed on to any of the 4 slots.

A few basic rules must be observed to prevent the addition of a podule causing interference with other extension cards. These rules will be become apparent from the description of the circuit diagram found in Fig. 2.

To begin with, the buffering of address, data and control lines is good practice to reduce the load on the respective computer buses, and to prevent digital interference generated on a podule upsetting the operation of the computer.

The databus is buffered by IC_{17}, an octal bus transceiver Type 74HCT245. The data direction can be reversed with the aid of signal R/W taken from the podule bus. The address bus and some signals on the control bus are buffered by IC_{15} and IC_{16}.

There are no address lines A0 and A1 because the ARM is a 32-bit processor that reads and writes one dataword as four bytes at a time. In practice, this means that the two least significant address lines are always low. To keep the PCB design as simple as possible, bidirectional buffers are permanently wired for one-way traffic.

Pin	ROW A	ROW C	
1	0 V	0 V	ground
2	LA[15]	–5 V	supply
3	LA[14]	0 V	ground
4	LA[13]	0 V	ground
5	LA[12]	*reserved*	
6	LA[11]	$\overline{MS}$	MEMC Podule Select
7	LA[10]	*reserved*	
8	LA[9]	*reserved*	
9	LA[8]	*reserved*	
10	LA[7]	*reserved*	
11	LA[6]	*reserved*	
12	LA[5]	$\overline{RST}$	reset
13	LA[4]	PR/$\overline{W}$	read/not write
14	LA[3]	$\overline{PWB}$	write strobe
15	LA[2]	$\overline{PRE}$	read strobe
16	BD[15]	PIRQ	normal interrupt
17	BD[14]	PFIQ	fast interrupt
18	BD[13]	*reserved*	
19	BD[12]	CI	I^2C serial bus clock
20	BD[11]	CO	I^2C serial bus data
21	BD[10]	$\overline{EXTPS}$	External Podule select
22	BD[9]	$\overline{PS}$	Simple Podule select
23	BD[8]	$\overline{IOGT}$	MEMC Podule handshake
24	BD[7]	$\overline{IORQ}$	MEMC Podule request
25	BD[6]	$\overline{BL}$	I/O data latch control
26	BD[5]	0 V	supply
27	BD[4]	CLK2	2 MHz synchronous clock
28	BD[3]	CLK8	8 MHz synchronous clock
29	BD[2]	REF8M	8 MHz reference clock
30	BD[1]	+5 V	supply
31	BD[0]	*reserved*	
32	+5 V	+12 V	supply

Fig. 1. Signals on the A and C rows of the 64-way podule connector.

Address decoding on the podule is done by PAL (programmable logic array) IC_{12} and decoder IC_{13}, a Type 74HCT139. The PAL is available ready-programmed. Circuit IC_{13} supplies the address selection signal for the VIA (versatile interface adapter) Type 6522, the ACIA (asynchronous communications interface adapter) Type 6850, and the ADC (analogue-to-digital converter) Type ZN427 in the sound sampler circuit. The combination of the PAL and the 74HCT139 supplies both the START OF CONVERSION signal and the READ signal for the ADC.

The INT signal, finally, is used to convey information on interrupt requests to the motherboard. If a read command is issued with INT selected, the status of IRQ and FIRQ is put on the databus via buffers N_7 and N_8. The computer requires this status information to identify the podule that generated the interrupt.

Apart from functioning as an address decoder, the PAL also converts the 8 MHz clock on the bus into a clean 4 MHz signal. Bistable FF_1 in IC_5 divides this 4 MHz signal down to 2 MHz, after which it is yet again divided by two, this time by the PAL. The resultant 1 MHz signal is required at several circuit locations.

Further tasks of the PAL are the synchronisation of signals BL and $\overline{PS}$ to the clock, and, lastly, the conversion of bus signal R/$\overline{W}$ into separate $\overline{R}$ (read) and W (write) signals that depend on PS.

The other bistable in IC_5, FF_2, is used to generate the clock signal for the 6850. The clock signal is 500 kHz in this case to enable the ACIA to communicate at 31.25 Kbaud, the standard serial data rate for MIDI equipment.

EPROM IC_{14} is addressed in a fairly unconventional manner, but there are cogent reasons for doing so. Since control lines V_{PP} and PGM are connected to the VIA, the user has the possibility to build an EPROM programmer starting from this socket. The software that copies the EPROM contents to the computer memory is not affected by the EPROM, but does need it. This is because the maximum permissible size of an EPROM address block on a (memory) podule is only 4 KBytes.

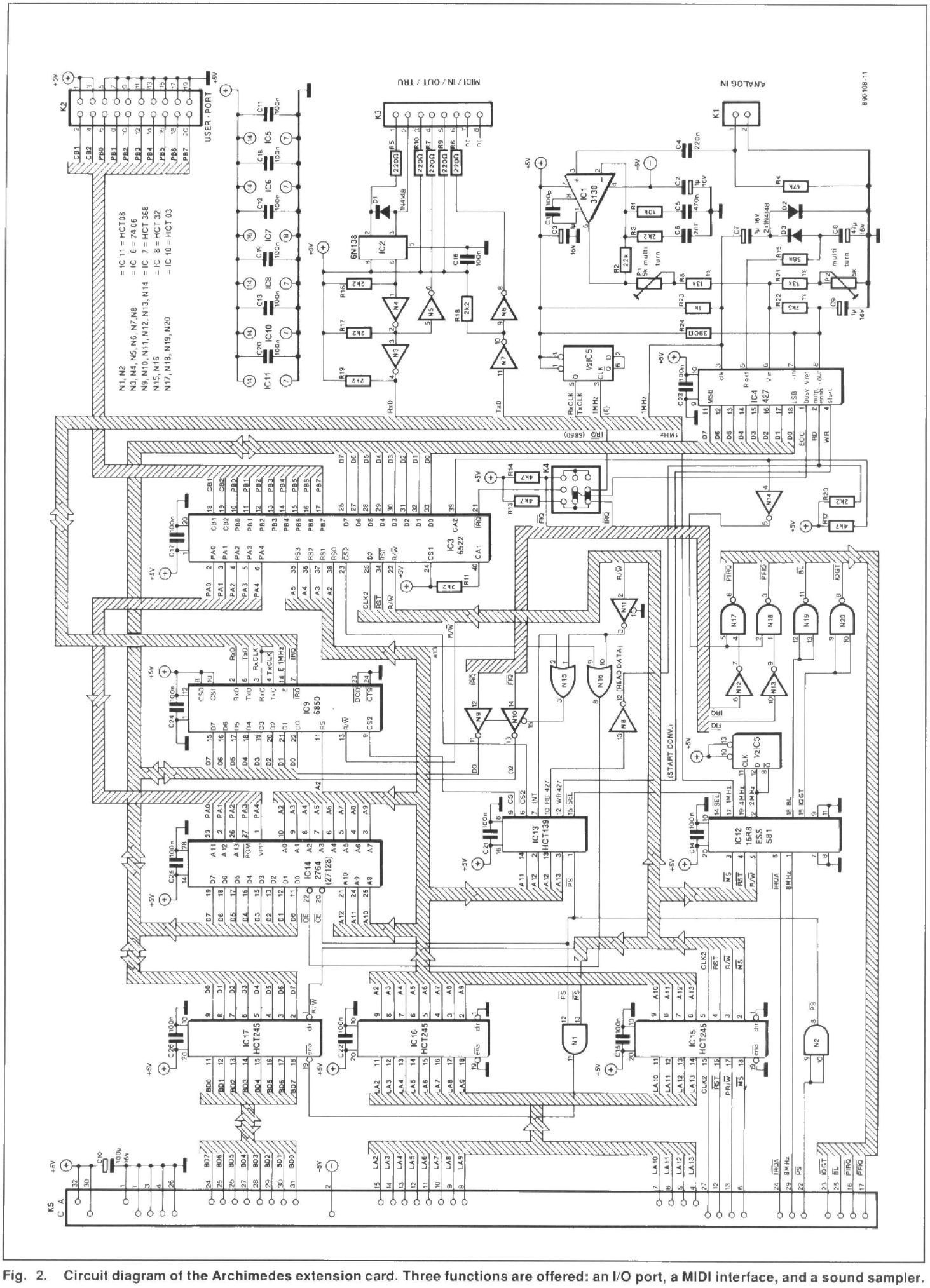


Fig. 2. Circuit diagram of the Archimedes extension card. Three functions are offered: an I/O port, a MIDI interface, and a sound sampler.

When the EPROM is paged, it is divided into blocks to meet this condition while allowing a total amount of software much larger than 4 Kbyte to be held.

Gates N_{13} through N_{16} are used to pass a number of signals to the motherboard. Lines IRQ and FIRQ signal the presence of interrupt service requests to the computer, IOGT is used for podule handshaking, and BL for controlling the I/O data latch.

Three in one

The podule contains 3 interfaces: sound sampler, MIDI interface and user port. The latter is the simplest. It is compatible with that used on the BBC-B and Master computers, and allows the same FX commands to be used for its control.

The MIDI interface is intended to accept Acorn's MIDI upgrade kit AKA15, which is sold separately as an add-on to the I/O podule by authorized retailers. Connector K_3 corresponds to the MIDI connector on Acorn's I/O podule, so that the set of DIN connectors is simple to use with the present podule. Unfortunately, the MIDI THRU connection available on the PCB is not used by the connector set. On K_3, the MIDI input is between pins 1 and 2, the MIDI THRU output between pins 3 and 4, and the MIDI output between pins 5 and 6 (also refer to Fig. 3). This means that a MIDI THRU output is only available if you use your own set of

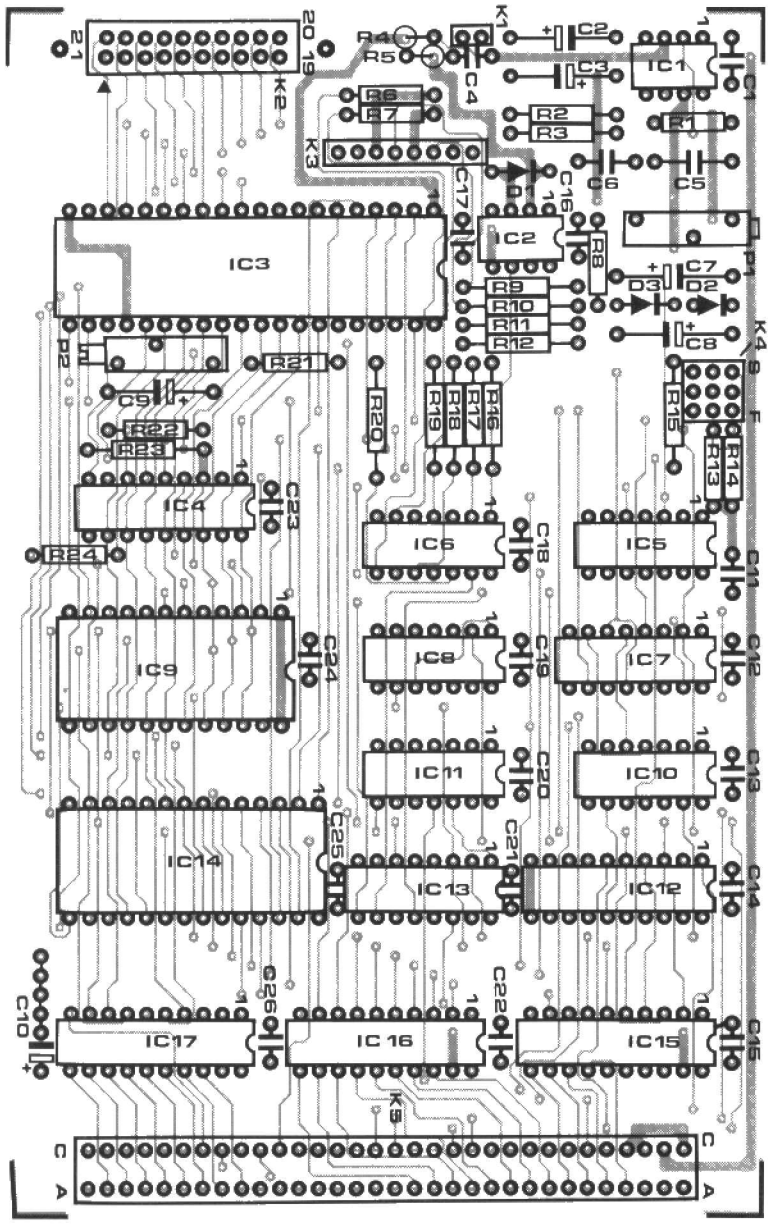


Fig. 3. Component mounting plan of the double-sided, through-plated printed circuit board for the extension card.

Parts list

Resistors:
R_1 = 10k
R_2 = 22k
R_3;R_{11};R_{16} – R_{20} = 2k2
R_4 = 47k
R_5;R_6;R_7;R_9;R_{10} = 220Ω
R_8;R_{21} = 13k0
R_{12};R_{13};R_{14} = 4k7
R_{15} = 56k
R_{22} = 7k5
R_{23} = 1k0
R_{24} = 390Ω
P_1;P_2 = 5k0 multiturn preset

Capacitors:
C_1 = 100p
C_2;C_3;C_7;C_9 = 1µ0; 16 V
C_4 = 220n
C_5 = 470n
C_6 = 2n7
C_8 = 47µ; 16 V
C_{10} = 100µ; 16 V
C_{11} – C_{26} = 100n

Semiconductors:
D_1;D_2;D_3 = 1N4148
IC_1 = 3130
IC_2 = 6N138 +
IC_3 = 6522
IC_4 = ZN427
IC_5 = 74HCT74
IC_6 = 7406 +
IC_7 = 74HCT368
IC_8 = 74HCT32
IC_9 = 6850 +
IC_{10} = 74HCT03
IC_{11} = 74HCT08
IC_{12} = 16R8 PAL (ESS 581)
IC_{13} = 74HCT139
IC_{14} = 27128 +
IC_{15};IC_{16};IC_{17} = 74HCT245

Miscellaneous:
K_1 = 2-way pin header.
K_2 = 20-way angled header with eject handles.
K_3 = 8-way SIL pin header.
K_4 = 3×3 pin header block.
K_5 = 64-way male PCB connector (A-C row).
Qty 2: jumper.
Qty 2: 5-way DIN socket +.
PCB Type 890108 (see Readers Services page).
Sound sampler control program ESS 105 (see Readers Services page).

+ in AKA15 kit from Acorn Computers Ltd.

DIN connectors.

The essential part in Acorn's MIDI upgrade kit is, of course, the EPROM that contains all support software for a MIDI interface and a user-port. If required, the other parts in the kit may be purchased separately. The EPROM is required for the I/O port and the MIDI interface, not for the sound sampler which is controlled by its own software.

The MIDI interface with its 6850 ACIA and 7406 open-collector driver is standard and could hardly be simpler. The 6850 divides the clock frequency of 500 kHz by 16 to arrive at the standardized MIDI data rate of 31.25 Kbits/s. The MIDI signal at the TXD output of the 6850 is inverted by N_7 before it is converted into a current-loop signal by N_6. Optocoupler IC_2 functions as the MIDI receiver device to guarantee electrical isolation of connected instruments. The digital serial signal is available at the output of the optocoupler. Gate N_5 converts the signal into a current loop again, creating a MIDI THRU connection. Gate N_3 buffers the serial signal and feeds it to the ACIA.

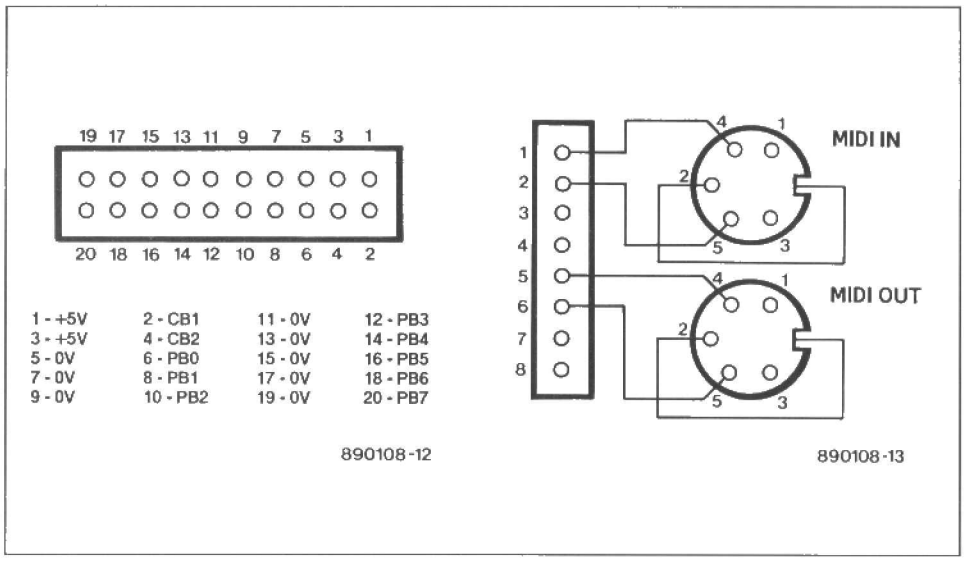


Fig. 4. Pinning of connectors K2 (I/O port) and K3 (MIDI port).

Digital sounds

The last and most extensive interface on the podule board is the sound sampler. By virtue of its advanced system architecture, the Archimedes is capable of direct conversion of digital samples to sound. In contrast with other computers, the Archimedes does not contain an FM synthesiser or chip for sound synthesis. The control system has available 8 digitized sounds that may be used by the computer. The present sound sampler allows quite a few sounds to be added to this basic collection.

The software developed for this part of the podule is capable of converting a sound sample into a relocatable module which, after being placed into memory, adds another synthesised sound to the computer's 'repertoire'.

Before a sound can be generated by the computer, an analogue (audio) signal must be digitized and converted into a block of logarithmic data that can be understood and processed by the computer. The analogue-to-digital conversion is carried out in hardware by the ADC on the podule, and the data compilation in software by the program available for this project.

The analogue input signal is amplified by IC_1, a Type CA3130 BiMOS opamp, and is passed through a pre-emphasis circuit that compensates for the non-linear response of the filters in the computer. Advanced users may find it useful to experiment with the component values of networks R_3-C_6 and R_1-C_5. The output signal of the opamp is fed to the ZN427 via P_2 and R_{21}. The ADC from Ferranti is simple to use by virtue of its internal reference source and TTL-compatible output. Also, its relatively short conversion time of 10 µs allows a sampling frequency of 73 kHz to be achieved. Preset P_1 is used to adjust the DC offset to 2.56 V, and P_2 to adjust the input volume. The optimum drive level for the sound sampler is 0 dB.

Construction

The double-sided, through-plated printed circuit board measures of 10x16 cm (Eurocard size). The component mounting plan is shown in Fig. 3.

Start the construction with mounting connectors K_2 and K_3 by means of nuts and bolts. Those used for securing K_2 also serve to fit, at a later stage, the metal bracket on to the board.

Solder all parts, with the exception of the EPROM, direct on to the board. By mounting the EPROM in an IC socket, the possibility is created to use the socket as the basis for an EPROM programmer at a later stage.

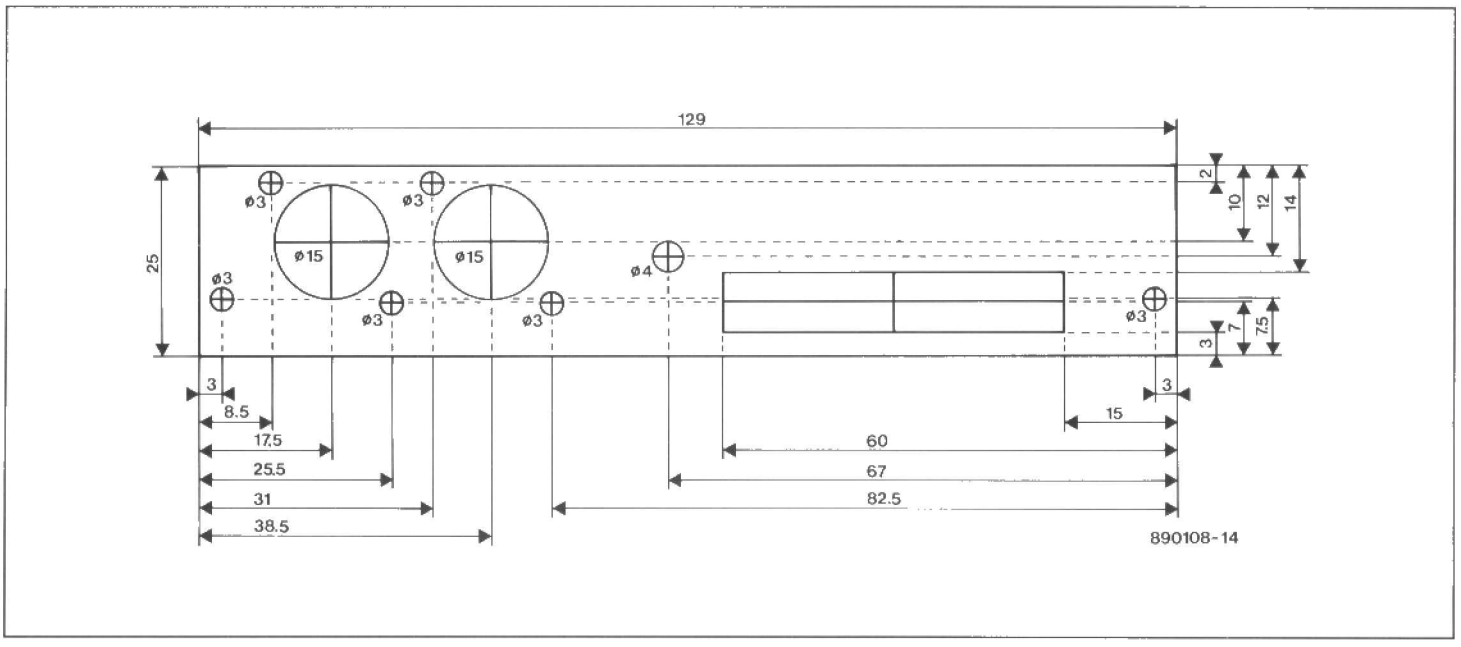


Fig. 5. Constructional drawing of the PCB-mounted aluminium bracket that holds the MIDI, AF input, and I/O port sockets.

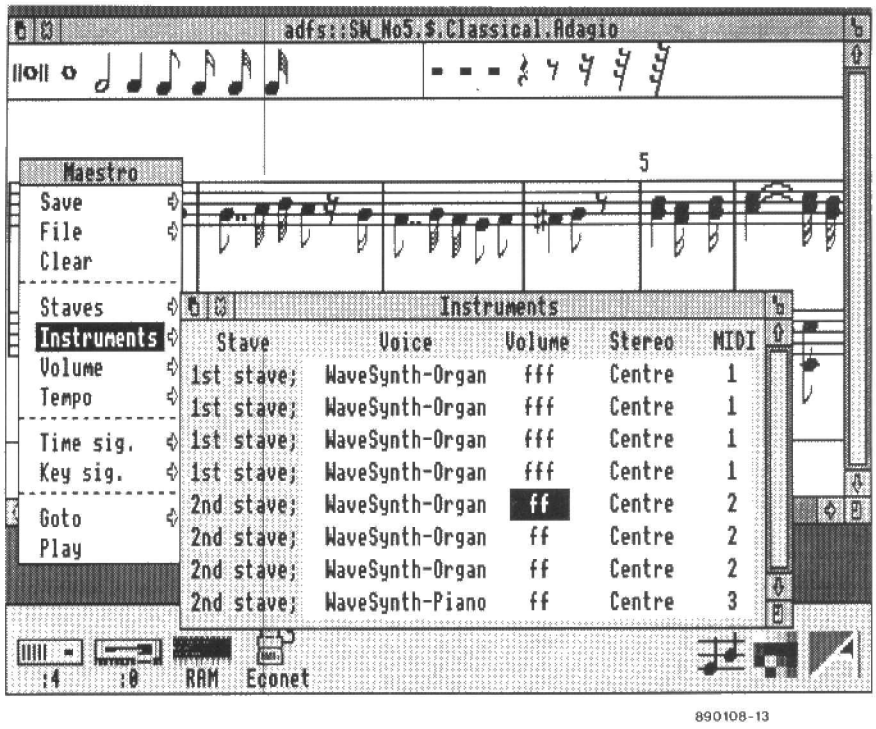


Fig. 6. Maestro shows that a number of MIDI channels are available, and lists the sampled signals that are ready for use as new modules.

Next, construct the metal support bracket. Cutting and drilling details are given in the drawing of Fig. 5. Use two M3 nuts to secure the bracket on to K_2 and the PCB. Simply omit the MIDI sockets if this part of the extension card is not used.

Finally, fit two jumpers on to pin header K_4. Both the ZN427 and the 6850 are connected to the slow interrupt, indicated by jumper position S. The user is free to decide whether or not the 6522 is connected to this interrupt line as well. The interrupt line of the 6850 must not be connected if the MIDI interface is not used.

On completion of the population work, check all part values and positions against the Parts List and the component overlay.

Set the two multiturn presets to the centre of their travel. Insert the card into a free podule slot, and switch the computer on. Type command *MODULES to check that the system has found two new modules: the I/O module that supports the user port, and the MIDI module.

Run an initial test on the MIDI module by starting Risc-OS application MAESTRO. A new column named MIDI must be found after selecting the 'instruments' option — see the Postscript screendump in Fig. 6. The sounds captured with the sampler on the extension board are ready for loading into the memory for use with MAESTRO.

Connect a voltmeter to pin 6 of IC_4, and adjust P_1 for a reading of 2.56 V. Preset P_2 can not be aligned without the help of the sound sampler control program supplied on disk (ESS 105). When this program is run, it uses the computer screen to show the applied signal in digitised form. The preset is then adjusted until the maximum usable input sound level is achieved without running into clipping or distortion.

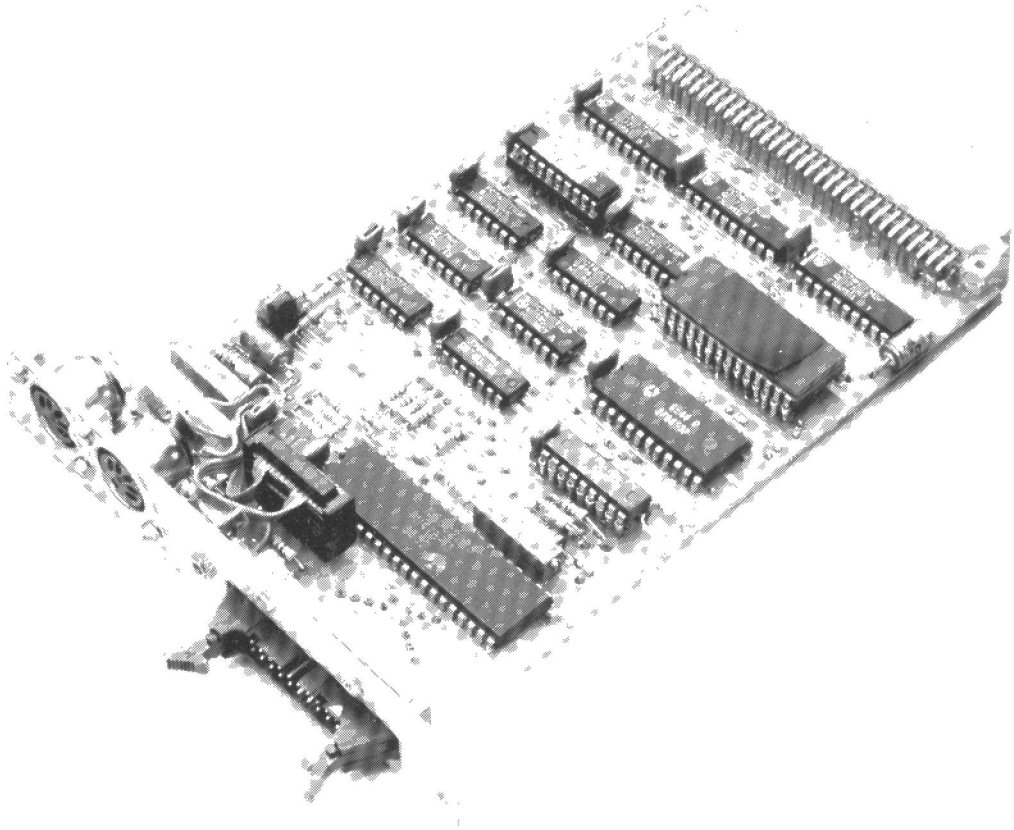
The software for this project is available on 3½-inch diskette only under order number ESS 105.

The printed-circuit board (890108), the programmed PAL (16R8; IC12) and the program diskette (ESS 105) are offered at a special package price under order number **890108-9**.

For details on ordering these items, please refer to the Readers Services page elsewhere in this issue.

The professional version of the software for the extension card may be obtained from

E.C.D. bv • Voldersgracht 26 • 2611 EV Delft • Holland. Telephone: +31 15 147643.



FERRITE LOOP AERIAL FOR THE 40 METRES BAND

R.Q. Marris G2BZQ

The ferrite rod aerial is typically associated with MW/LW radios, but it can be used on HF as well. Following a number of experiments with ferrite rod aerials, this article describes a highly directive type that covers the frequency range from 5,000 to about 8,300 kHz, spanning the popular 40 metres amateur band.

The ferrite rod aerial found in MW/LW radios is usually made of a manganese-zinc material. The aerial described here uses a different material, a nickel-zinc alloy, and has a diameter of 0.5 inch. It can have a length of 7.5 inch, or 15 inch if two rods are glued end to end.

The main purpose of using a ferrite rod aerial is to exploit its directivity to suppress interference. To obtain the best possible Q (quality) factor, the inductance must be wound at either side of the rod centre. Also, the spacing between the turns and, most importantly, between the turns and the core, contribute to the selectivity. The last factor has to be arrived at largely by experiment, as little published material is available.

The ferrite rod

The usual technique is to use an inductor, wound on the ferrite rod, and resonate this by a variable capacitor (VC) of somewhere between 250 pF and 750 pF, depending on the frequency range. This technique has previously been used, on the HF bands, to achieve the widest possible frequency range. Experiments, however, showed that the technique produces a variation in sensitivity over the frequency range, particularly when the tuning capacitor is approaching maximum capacity. On the medium and long-wave bands this matters little, but on the HF bands it is more noticeable if serious tests are conducted. The effect was investigated further with a view to obtaining the optimum aerial performance over a comparatively narrow frequency range, such as one of the amateur radio bands — in this case the 40-meter or 7 MHz band (7,000 – 7,300 kHz).

Critical factor

The circuit diagram of the ferrite loop aerial is shown in Fig. 1. It consists of a nickel-zinc ferrite rod inductor, L_1, in a balanced circuit tuned by VC, the variable capacitor. A coupling coil, L_2, connects a low-impedance feed-line to the aerial input on the communications receiver (RX). Coil L_3 enables an external aerial to be connected, and is discussed later.

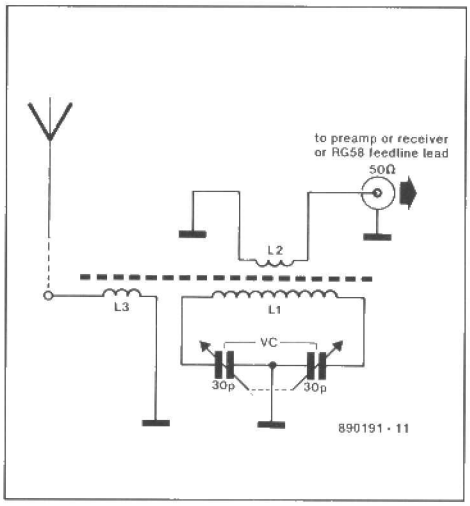


Fig. 1. Circuit diagram of the ferrite loop aerial for the 40-metres amateur radio band.

The critical factor in the ferrite loop aerial is to keep the VC as small as possible whilst ensuring that L_1 has a high Q (quality) factor. To obtain a high Q factor, it is necessary to have the optimum gap between the turns of the winding and the ferrite core. A simple, traditional, method to obtain the correct gap is to use PVC or polythene covered wire, and to vary the outer diameter of the wire covering with respect to the rod. This method also provides spacing between turns, ensures simplicity of construction, and eliminates the need of using a coil former, which is virtually impossible to obtain especially in alternative wall thicknesses.

The wire used for the 40-m ferrite aerial is single-strand 1/0.6 mm PVC-covered with an overall diameter of 1.2 mm. Similar wire is available with an outer diameter of about 1 mm, but should not be used for this project. The variable capacitor must be a good quality, 2-gang 30 pF per section, airspaced type.

Construction

The rod and winding assembly details are shown in the drawing of Fig. 2. First, wind L_1 central on the rod using 31 turns close-wound. Secure the wire ends with tape as shown in the drawing. Next, cover L_1 with a double layer of 10-mm wide postcard, which is secured with a piece of double-sided sticky tape. Close-wind the 3 turns of L_2 over the centre of L_1, and twist the wire ends together. Finally, close-wind the 4 turns of L_3, starting at a distance of 37 mm from the edge of L_1.

The aerial assembly is shown in Fig. 3. It consists of a heavy softwood base and two verticals, the cross-section of which could be reduced if hardwood were used. The wooden blocks are secured together as shown, and given a teak colour with a spirit stain. Plastic-coated Terry clips are screwed near the top sides of the verticals to support the ferrite rod. The Terry clips are preferred to the usual chrome clips because they do not chip the ferrite. The heavy base is required to prevent the

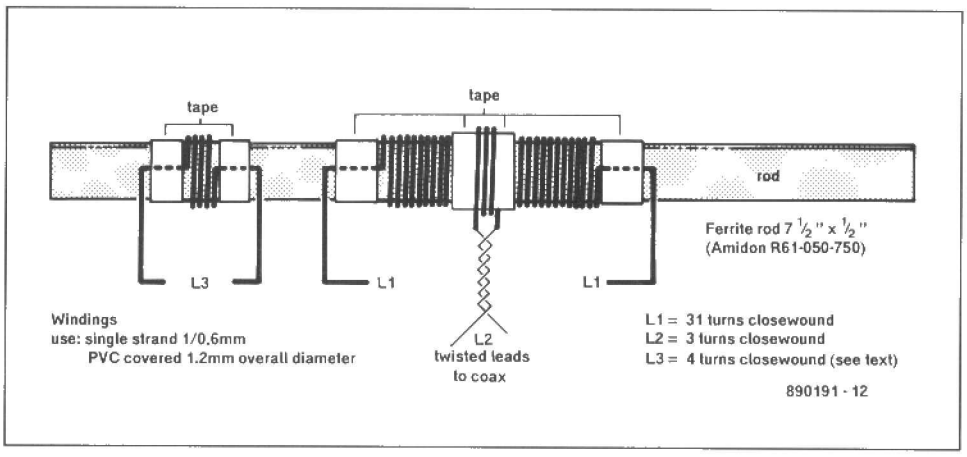


Fig. 2. Winding and assembly details of the ferrite rod.

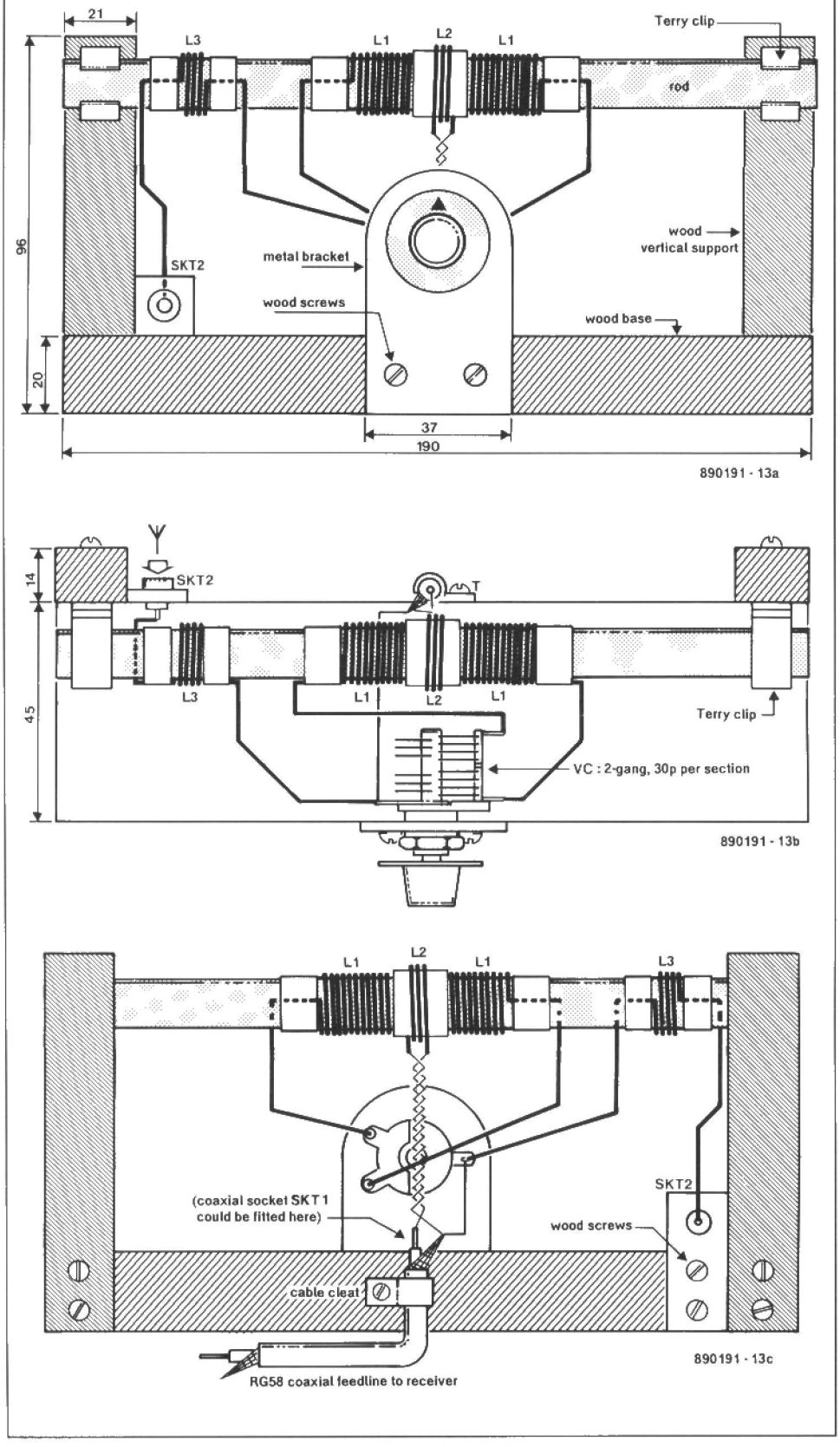


Fig. 3. Construction and assembly details of the ferrite-rod loop aerial for 40 metres.

spring in the coaxial cable moving the assembly.

Mount the variable capacitor on a metal plate, and at angle so that the connecting tags on the stators are as near as possible to L_1 to keep the leads short.

Connect the twisted ends of L_2 to the coaxial feedline (RG58) either via socket Skt_1 as shown in the circuit diagram, or by direct connection as illustrated in Fig. 3. If the receiver has an input impedance of 75 Ω, TV coax cable must be used instead of RG58.

Solder all earth connections to the metal body of the variable capacitor.

Take the outer end of L_3 to the rear-mounted socket Sk_2; the other wire end goes to earth. Coupling coil L_3 enables an end-fed aerial to be connected, when required, in which case the combination VC-L_1 acts as an aerial tuning unit (ATU). This avoids the necessity of plugging and unplugging alternate aerials at the input of the receiver. Socket Sk_2 could be replaced with a simple change-over switch. The specified number of turns of L_3 is suitable for a 9-meter long, end-fed aerial, and may have to be changed by experiment if a much longer wire is used.

Parts list

Ferrite rod:
Type R61-050-750. Length: 7½-inch. Diameter: ½-inch. Amidon Associates • 12033 Otsego Street • North Hollywood • California 91607 • U.S.A.

Wire:
Single-strand 1/0.6 mm, tinned 0.6 mm conductor covered by 0.3 mm wall thickness PVC. Overall diameter 1.2 mm. Type CBL/EW1/WHITE. Marco Trading • The Maltings • High Street • Wem • Shrewsbury SY4 5EN.

Variable capacitor:
Good quality 2-gang 30 pF per section (remove padding capacitors if fitted).

Sockets:
Skt_1 = coaxial socket, e.g. SO-239 (Amphenol).
Skt_2 = wander socket.

Miscellaneous:
Wood, screws and masking tape.

Performance, operation and directivity

The ferrite-loop aerial covers the frequency range from 5,000 kHz to 8,300 kHz, spanning the required 7 MHz amateur radio band, with some adjacent broadcasting stations which are useful test references.

Operation is simple: tune the receiver to the 7 MHz band and tune the variable capacitor for maximum noise level. If required, re-tune on individual signals. The aerial must be rotated for maximum signal strength, which is obtained at the 'flat side' of the loop. Minimum signal occurs at the ends. Minor rotation of the aerial may help, in many cases, to eliminate interference from other stations, as well as static and man-made electrical noise. The nulling of the aerial is quite pronounced. Also, being a narrow-band type, the ferrite loop aerial produces much less noise than an external aerial.

The author uses the ferrite loop aerial with a modified receiver with high RF gain. Depending on your location and your receiver's sensitivity specifications, it may be necessary to insert a preamplifier between the aerial and the receiver input.

8098 EVALUATION BOARD

by J.M. Wald

Many microprocessor-based designs require, in addition to RAM and ROM or EPROM, several peripheral ICs to interface to 'The Real World'. For instance, it is often necessary to provide both an analogue-to-digital converter and a serial port. A simpler and more efficient system can be designed with the use of one of the many 'microcontrollers' that combine a processor, RAM, several peripherals and even ROM or EPROM on a single chip

The Intel 8096 family is a set of software-compatible 16-bit microcontrollers with an 8- or 16-bit bus. The members of the 8096 family have a powerful 16-bit CPU and a number of on-chip peripherals. The majority of the 16-bit bus devices can generate either 8- or 16-bit bus cycles on a cycle-by-cycle basis. The most important members of the 8096 family are:

8098 The 8-bit bus HMOS version, packaged in a 48-pin DIP. The 8098 has a 4-bit I/O port and a 4-channel analogue-to-digital converter.

8097BH A 16-bit bus HMOS version, packaged in 68-pin PGA or 68-pin PLCC. The 8097BH has two 8-bit I/O ports and an 8-channel analogue-to-digital (A-D) converter.

8797BH This is identical to the 8097BH, but has in addition 8 K of EPROM, and is packaged in a 68-pin PGA or 68-pin LCC.

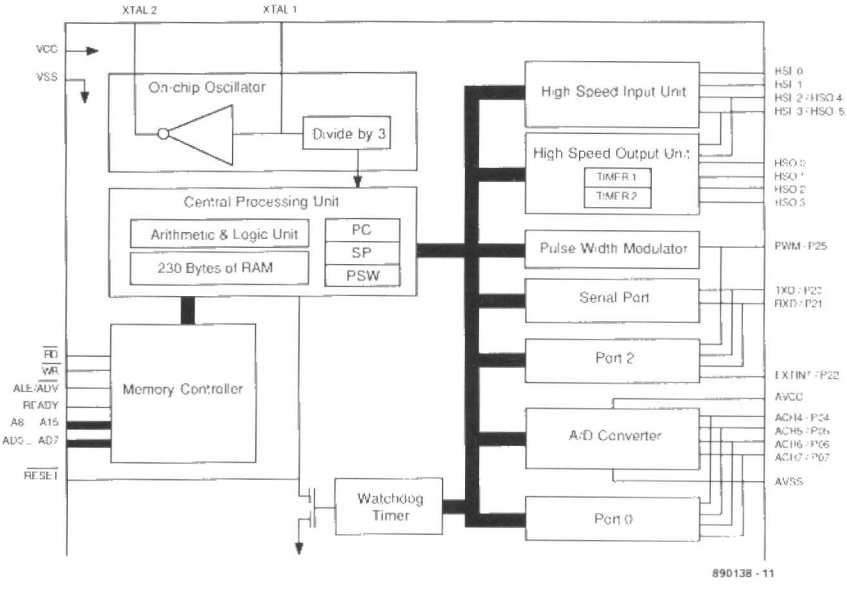
80C196 This is the 16-bit bus CHMOS version, packaged in a 68-pin PLCC. The 80C196 has two 8-bit I/O ports and an 8-channel A-D converter. The CPU on the 80C196 is at least 50% faster than on the other 8096 devices, and accepts several additional instructions. Moreover, the 80C196 may be placed in a low-power mode.

87C196 This is identical to the 80C196 but has additionally 8 K of EPROM and is packaged in a 68-pin LCC.

In addition, all 8096 devices contain 230 bytes of RAM, a pulse-width modulated output, a 16-bit event counter, four high-speed inputs, six high-speed outputs, four software timers, a serial port, a baud rate generator, an an on-chip oscillator.

The evaluation board for the 8098 described in this article has space for 8–48 K of EPROM and 32–64 K of static RAM. There are three RS232 ports for connexion to the user's application, a printer and a host computer. The monitor program (see Fig. 7) may be used to allow the host computer to control the board and send code for execution in the evaluation board's RAM.

Figure 1 – 8098 Block Diagram



In addition, the board has three expansion connectors. One of these carries the system bus, another a number of 8098 I/O lines, and the third has two 8-bit I/O ports from a PIO (parallel input/output).
The board requires a simple external power supply providing +5 V and ±9 V. The +5 V rail is supplied to all three connectors to enable other boards to be powered directly from the evaluation board.

The 8098 consists of a central processing unit (CPU) connected to a memory controller and various peripherals, all synchronized by an on-chip oscillator as shown in Fig. 1.

The 8098 on-chip oscillator can be used with a parallel resonant crystal with a fundamental frequency of 6–12 MHz. Two external capacitors provide the correct loading for the crystal. The oscillator output is divided by three to form the internal clock. A period of the internal clock is known as a 'state'.

The memory controller is used to prefetch instructions and to access operands

Figure 2 – 8098 CCB Format

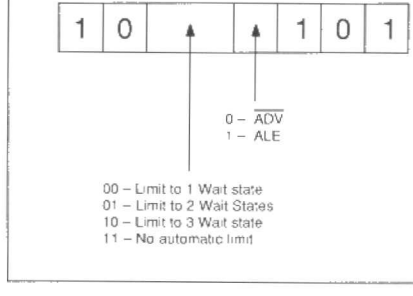
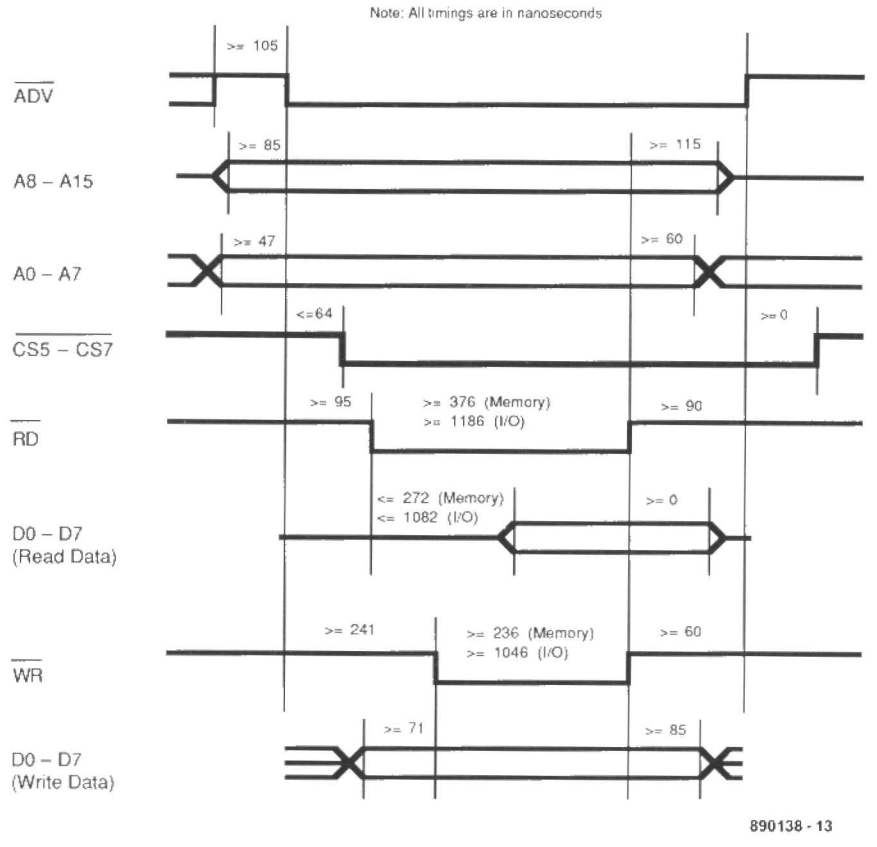


Figure 3 – 8098 Evaluation Board Bus timing



held in external memory. Immediately after the $\overline{\text{RESET}}$ input is negated high, the memory controller fetches the 'chip configuration byte' (CCB) from location 2018 hex (see Fig. 2).

The CCB specifies a limit for the number of wait-states to be allowed in memory cycles and also specifies the type of bus control signals generated. Memory cycles normally take two states. However, if the READY input is asserted low, wait-states are inserted into the memory cycle until either READY is negated high or the limit specified in the CCB is reached.

Note that if the CCB specifies a wait-state limit, it is not necessary to externally negate READY. This feature is used in the evaluation board. The 8098 is limited to a maximum of three wait-states or a delay of 1 µs, whichever is shorter, since internal dynamic logic will begin to lose information after this time.

Figure 3 shows the detailed bus timings for the evaluation board. The 8098 uses a multiplexed address and data bus. The upper eight address lines, A8–A15, are always available, but the lower eight address lines, A0–A7, use the same pins as the eight data lines, D0–D7.

During the first part of a memory cycle, the low byte of the bus carries the address and only after the address has been latched externally is the bus used for data. A bit in the CCB selects whether ALE or $\overline{\text{ADV}}$ is to be generated as the address latch signal.

ALE is a signal that is normally low, but is asserted high when a valid address is present on the multiplexed address/data pins. $\overline{\text{ADV}}$ is a signal that is normally high, including when valid address information is available, but is asserted low during memory cycles. The evaluation board uses $\overline{\text{ADV}}$ as the address latch signal, and this signal is also used as a factor in the memory selection circuitry.

Read cycles use an active low strobe, $\overline{\text{RD}}$, to enable data from external devices on to the data bus. Write cycles use an active low strobe, $\overline{\text{WR}}$, that is asserted once valid data appears on the bus, and is negated before data is removed from the bus. The write strobe is considerably shorter than the read strobe and is asserted low in the memoray cycle later than the read strobe.

The 8098, in common with other Intel processor, stores multi-byte data in such a way that the least significant byte is held in the lowest address, and the most significant byte is held in the highest address. Word data must be held at an even address and long-word (32-bit) data must be held at an address divisible by four. However, unlike most other processors, the CPU on the 8098 uses the on-chip zero-page RAM, and not the registers, as working storage. For convenience, all zero-page locations are known as registers. This means that the 8098 effectively provides the equivalent of 230 byte registers or 115 word registers. Of the other 26 zero-page locations, two form the zero register (a register that always contains zero), two form a 16-bit stack pointer (SP), and the remainder control the on-chip peripherals and are known as special function registers (SFRS).

Figure 4 – Register Map

Address	Register		
001C	AX	AL	AH
001E	DX	DL	DH
0020	BX	BL	BH
0022	CX	CL	CH

The stack pointer points at the last item on the stack and is always even. As a result, only word and long-word data can be pushed on to the stack. The stack grows towards low address and can be held anywhere in RAM. Programs execute more quickly if the stack or data is held in zero-page RAM.

The advantage of this architecture is that the programmer can use any zero-page location as a data register, an index register or a variable without the need to transfer the contents of the location to a CPU register to perform operations on the contents of the location. For example, the contents of two locations can be multiplied together without the need of an intermediate accumulator. All register instructions can operate equally on all zero-page RAM locations, including SP, the zero register and the SFRS.

Intel suggest a convention for register allocations in programs as shown in Fig. 4. The locations from 1C hex to 23 hex are used as four named word registers: AX, DX, BX, and CX. In addition, the low byte of AX is called AL, and the high byte of AX is called AH.

Similarly, the other registers are divided into DL, DH, BL, BH, CL and CH. Note that these are not real registers, despite their similarity to 8086 register names, but merely symbolic names allocated to zero-page locations. Note also that AX and DX are adjacent and may be combined to form AXDX, a long-word register. The other locations in the zero-page are free to be allocated as additional 'registers' or as data RAM.

In addition to the zero-page RAM, the CPU also contains a program counter, PC, and a processor status word, PSW. The low byte of the PSW contains the interrupt mask register, which is used to selectively enable interrupts from the various on-chip interrupt sources. The high byte of the PSW contains the condition code flags: zero, Z; negative, N; overflow, V; overflow trap, VT; carry, C; interrupt enable, I; and sticky, ST. The flags function in a manner similar to those on other processors, with the exception of the N, VT and ST flags.

The N flag is set if the sign of the true result is negative and is cleared if the sign of the true result is positive or zero. The true result is the obtained when the operation is performed to sufficient precision to avoid overflows. This is different from other processors that set their N flags to the sign of the actual result obtained, even if an overflow occurs. This change affects

the conditional jump instructions required after signed arithmetic and comparisons. In particular, the signed conditional jump instructions need only to test the N and Z flags and can ignore the V flag except for explicit overflow tests.

The VT flag is set whenever the V flag is set, but it is cleared by a CLRVT, JVT or JNVT instruction. The CLRVT instruction simply clears the flag, whereas JVT and JNVT test the state of the VT flag and jump if the flag is set or clear as appropriate. This allows a test for overflow to be made at the end of a series of arithmetic operations, rather than after each operation.

The ST flag is affected by shift right instructions and is set if any of the bits in the original operand beyond the last bit shifted out were one: otherwise the ST flag is cleared. For example, if a register is shifted right by five bits, the ST flag will be set if any of the least significant bits of the original operand were one, otherwise the ST flag will be cleared.

The ST flag is used to implement an improved rounding algorithm as compared with the conventional method of rounding fractions below 0.5 towards zero and fractions greater than, or equal to, 0.5 away from zero. The conventional algorithm rounds towards zero if the carry flag is clear, and rounds away from zero if the carry flag is set. The improved rounding algorithm is similar to this, except that fractions equal to 0.5 are rounded to the nearest even number. The fraction is below 0.5 if the C flag is clear; it is equal to 0.5 if the C flag is set and the ST flag is clear; and it is above 0.5 if both the C and the ST flags are set.

The 8098 has five addressing modes: immediate, register direct, register indirect, indexed and relative. The location indicated by the addressing mode must conform to any alignment restrictions required by the instruction size. The majority of 8098 instructions can use any addressing mode, except relative, and the type of addressing mode is encoded in the least significant two bits of the op-code. However, single operand arithmetic, and logical and shift instructions, such as CLR, NEG and SHRA, are restricted to using register direct mode.

Relative addressing mode is used only by jump and call instructions. There are no absolute jump or call instructions: as a result it is very easy to make programs relocatable.

The immediate mode is used to specify a constant 8- or 16-bit data item held in the object code following the op-code. The least significant two bits of the op-code are 01.

The register direct mode is used to specify a zero-page location as an 8-bit address held in the object code. The least significant two bits of the op-code are 00. If the instruction is word sized, the zero-page address must be even.

The register indirect mode is used to access operands held anywhere in memory with a zero-page word location used as a pointer. The least significant two bits of the op-code are 10. The object code contains the 8-bit address of the word location used as a pointer. In a second form of the register indirect mode, known as register indirect with post-increment, the pointer is incremented after the operand has been accessed. The pointer is incremented by one for byte instructions and by two for word instructions. The processor distinguishes between the two addressing modes by the use of the least significant bit of the 8-bit pointer address. If the address is even, the mode is register indirect, otherwise it is register indirect with post-increment. In both cases, the address used to access the pointer is even.

The indexed addressing mode is similar to the register indirect mode, except that an 8- or 16-bit signed constant offset, held in the object code, is added to the pointer to form the address of the operand. The least signbificant two bits of the op-code are 11. It is n ot possible to combine post-incrementing with the indexed mode.

The use of an 8-bit constant is known as short indexed, while theat of a 16-bit constant is termed long indexed. The processor distinguishes between the two addressing modes by using the least significant bit of the 8-bit pointer address. If the address is even, the mode is short indexed, otherwise it is long indexed. Note that as in register indirect mode the address used to access the pointer is always even.

The extended addressing mode used in other processor to access locations outside the zero-page can be synthesized by the use of the long indexed mode, with zero as the address of the pointer and address of the operand as the 16-bit offset. This is possible because the zero-register always contains zero.

The relative addressing mode has three short forms: short, medium and long. The short form is used only by the conditional jump instructions and allows a jump to any location within –126 bytes to +129 bytes from the jump instruction. The medium and long forms are used by the jump and subroutine call instructions. The medium form allows a range of –1022 bytes to +1025 bytes, while the long form permits a range of –32766 bytes to +32769 bytes.

The instruction set has all the usual arithmetic and logical instructions, including multiplication and division instructions as shown in Fig. 5. The arithmetic and logical instructions require the destination operand to be held in a register; the source operand is specified with the use of any addressing mode except relative.

The add, subtract, multiply and logical-and instructions also have a three-operand form that allows two source operands and a separate destination operand. One source operand is is held in a register, while the other is specified with the use of any addressing mode except relative.The destination operand is always a register.

The add and subtract with carry instructions can clear the Z flag, but they can not set it. This ensures that the Z flag has the correct state at the end of a multi-precision addition or subtraction. All instructions have a byte- and a word-form, and the shift instructions also have a long-word form.

The NORML (normalize) instruction is a special shift instruction that can be used to speed up floating point routines. This instruction shifts the operand long-word register left until the MSB is one, and also returns the number of shifts performed in a separate destination byte register.

The instruction set contains a complete range of conditional jump instructions that can be used to test for the state of all the flags except I. It is possible to test for all six con ditions [<, <=, =, >=, >, <>] after both signed and unsigned comparisons with the use of the appropriate conditional jump instruction. The JBC and JBS instructions can be used to perform a jump if a bit in a register is clear or set.

The TRAP instruction performs a software interrupt and vectors to the address held in locations 2010 hex and 2011 hex. The RST instruction resets the processor and the SKIP instruction is a two-byte NOP.

Figure 5 – 8098 Instruction Set

Arithmetic	Logical	Program Transfer
Two & three operand instructions ADD ADDB SUB SUBB MUL MULB MULU MULUB	Two & three operand instructions AND ANDB	Conditional Jumps JC JNC JE JNE JV JNV JVT JNVT JST JNST JLT JGE JGT JLE JH JNH JBC JBS DJNZ
Two operand instructions DIV DIVB DIVU DIVUB CMP CMPB	Two operand instructions OR ORB XOR XORB	Unconditional Jumps SJMP LJMP BR
One operand instructions CLR CLRB EXT EXTB NEG NEGB INC INCB DEC DECB	One operand instructions NOT NOTB	Subroutine Linkage SCALL LCALL RET
Data Transfer	**Shifts**	**Miscellaneous**
LD LDB ST STB PUSH POP PUSHF POPF LDBSE LDBZE	SHLL SHL SHLB SHRL SHR SHRB SHRAL SHRA SHRAB NORML	CLRC SETC DI EI CLRVT NOP SKIP RST TRAP

On-chip peripherals

The high-speed output unit, HSO, consists of a 16-bit timer (TIMER1), a 16-bit event counter (TIMER2) and an 8-level command register.

TIMER1 may be read with the use of locations 0A hex and 0B hex, is incremented every eight states and is cleared on reset.

TIMER2 is cleared on reset by software or by a positive level on HSI0. Each level in the command register can hold a com-

mand programmed to be acted upon at a specified time relative to TIMER1 or TIMER2.

The command can set or clear one of six output pins, set one of four software timer status flags, clear TIMER2, or start the A-D converter. In addition, the command can generate an interrupt if required. As soon as a command has been acted upon, it is deleted from the command register. Note that two HSO outputs, HSO4 and HSO5, use the same pins as HSI2 and HSI3 of the high-speed input unit.

The high-speed input unit, HSI, can be programmed to look for transitions on any or all of four input pins, two of which are shared with the HSO unit. The unit can look for positive **and** negative transitions, positive transitions only, negative transitions only, or every eighth positive transition.

The HSI can look for different types of transition on different pins. When the HSI detects a valid transition, it records the value of TIMER1, together with a flag for each of the four pins, in a seven-level queue. The flag is set if a transition was detected on that pin, otherwise it is clear. The HSI can generate an interrupt when it detects a transition or when the queue is full. HSI0, one of the four HSI input pins, can generate an interrupt independently of the HSI when it receives a leading edge.

Note that HSI1, HSO0 and HSO1 are used in the evaluation board to implement the software serial ports. As a result, the user's application is not able to use either TIMER2 or these I/O pins.

The A-D converter can convert an analogue signal in the the range 0–5 V on any of four input channels to a 10-bit digital value. It has a built-in sample-and-hold, so that it is not necessary to maintain the input voltage throughout the entire conversion process. The converter uses a pair of power supply pins separate from the rest of the chip, so that an accurate and stable reference voltage can be used. However, the converter supply pins must always be connected even if the converter is not being used.

The A-D converter takes about 33 µs at a clock frequency of 8 MHz to perform a conversion, and can generate an interrupt as soon as a conversion has been completed. The conversion may be started immediately or after a delay with the aid of the HSO unit. The four input pins used by the converter are shared with Port 0.

The pulse-width modulated (PWM) output may be used to oujtput a pulse train with a programmable high level duty factor to a pin that is shared with Port 2, bit 5. The period of the pulse train is fixed at 256 states and the high-level duty factor may be varied from 0 to 0.996. At a clock frequency of 8 MHz, the pulse train has a period of 96 µs: the high period may be varied from 0 to 95.6 µs. The PWM pin may be buffered and used to drive devices such as motors, or it may be integrated and amplified to provide a true D-A converter.

The full duplex serial port can be used in synchronous or asynchronous mode. The baud rate is derived from an internal baud rate generator that is driven by the on-chip oscillator or by TIMER2. The baud rate generator divides the reference frequency to the desired baud rate with the aid of a programmable 16-bit divisor.

In the asynchronous mode, the port can operate at baud rates of up to 125 kHz with a clock frequency of 8 MHz. In synchronous modes, the port can operate at baud rates of up to 1 MHz with a clock frequency of 8 MHz. The serial port can be programmed to generate 8- or 9-bit data with or without even parity. If odd parity is required, it must be generated and checked by software. In the 9-bit data mode, the serial port can ignore all received characters whose MSB is clear. This can be used for multi-processor links to enable processors to ignore messages and only respond when they are sent an address character with the MSB set. The serial port can generate interrupts when characters are received and after characters have been transmitted. The transmit and receive data lines are shared with bit 0 and 1 of Port 2.

The 8098 has two 4-bit I/O ports. Port 0 is an input-only port that uses the same pins as the A-D converter. Bit 7 of port 0 can generate an interrupt on a leading edge. Port 2 has two output pins (bits 0 and 5) and two input bits (bits 1 and 2). Bits 0 and 1 are shared with the serial port and bit 5 is shared with the PWM output. Port 2 bit 2 is an input that can also generate an interrupt on a leading edge.

The watchdog timer is a 16-bit counter that can be used to reset the CPU automatically in the event of a major system error, for instance, executing code from non-existent memory. Once the watchdog timer has been started by the programmer, it is incremented every state until it overflows or is cleared by the programmer. Note that once the timer has been started, it is not possible for the programmer to stop it except by resetting the 8098.

When the timer overflows, it resets the chip by pulling the $\overline{\text{RESET}}$ input low. The short pulse on the $\overline{\text{RESET}}$ pin may be lengthened with the aid of a monostable and then used to reset other devices in the system.

In the event of a system error, it is most unlikely that a program will continue to clear the timer, and so the watchdog timer will overflow and reset the chip.

The interrupt system used by the 8098 is both simple and flexible. There are eight 16-bit interrupt vectors located at 2000 hex (see Fig. 6). Each interrupt vector has an associated interrupt pending bit and an interrupt mask bit. The eight mask bits are held in a register at location 8, and the eight pending bits are held in a register at location 9. The vectors and the associated pending bits are each assigned a priority level.

Whenever an interrupt occurs, the associated pending bit is set. If the corresponding mask bit is set, there are no interrupt pending bits of a higher priority and the I flag is set in the PSW: the processor then saves the current value of PC on the stack and jumps to the address held in the interrupt vector table of the appropriate interrupt service routine. Once the interrupt has been accepted and the jump taken, the associated interrupt pending bit is cleared.

The first instruction of the interrupt service routine must use the PUSHF instruction to save the PSW. Any other registers used by the routine must also be preserved. Note that because of the large number of registers it is not normally necessary to use those registers in the main program that are used in the interrupt routines, so that the overhead of saving and restoring registers during interrupts is usually avoided. The PUSHF instruction pushes the PSW on to the stack and then clears the PSW. This action disables all further interrupts as a result of clearing both the I flag and the interrupt mask register.

The interrupt mask register may be changed within the service routine to alter the interrupt priorities and to allow interruptable service routines. However, before interrupts are allowed again, the I bit in the PSW must be set. This mechanism permits the programmer to determine the priority between different interrupts sources completely.

The last instruction in the interrupt service routine before the RET (return) instruction uses the POPF instruction to reload the PSW, thus restoring the original state of the system.

The processor does not immediately accept interrupts after TRAP, EI, or POPF instructions, but instead delays accepting any pending interrupts until after the fol-

Figure 6 – Interrupt Vectors

VECTOR ADDRESS	INTERRUPT PENDING REGISTER BIT	VECTOR	PRIORITY LEVEL
2000	0	TIMER OVERFLOW	LOWEST
2002	1	A/D CONVERSION COMPLETE	
2004	2	HSI DATA AVAILABLE	
2006	3	HSO COMMAND ACTED ON	
2008	4	HSI.0 POSITIVE EDGE	
200A	5	SOFTWARE TIMERS	
200C	6	SERIAL PORT	
200E	7	EXTINT (P2.2 or P0.7)	
2010	None	TRAP INSTRUCTION	HIGHEST

lowing instruction has been executed. This ensures the execution of at least one instruction in the program before interrupts are accepted and also that the stack does not overflow as a result of data placed on it during the interrupt. In particular, the RET instruction at the end of the interrupt service routine will be executed before any pending interrupts are accepted.

It is also possible to set or clear bits in the interrupt pending register either to generate false interrupts or to cancel real interrupts. However, it is important that the interrupt pending register is modified with the aid of a single logical instruction. This will ensure that the 8098 does not change interrupt pending bits as a result of interrupts between the time the program reads the register and the time the modified value is written back again.

The construction and testing of the board will be dealt with next month.

Fig. 7.– 8098 Evaluation Board Monitor Hex Dump

```
2000 5F 27 65 27 6B 27 77 27 7D 27 83 27 8C 27 92 27
2010 98 27 FF FF FF FF FF FF 95 FF 27 FE FF FF FF FF
2020 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2030 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2040 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2050 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2060 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2070 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2080 E7 EC 04 E7 2D 09 E7 26 09 E7 38 09 E7 3C 09 E7
2090 C7 08 E7 B4 08 E7 67 08 E7 2E 07 E7 53 07 E7 3B
20A0 08 E7 6B 07 E7 8D 07 E7 A8 07 E7 C2 07 E7 F3 07
20B0 E7 1A 08 E7 35 08 E7 33 00 E7 38 00 E7 40 00 E7
20C0 4D 00 E7 6C 00 E7 7D 00 E7 9F 00 E7 B0 00 E7 E6
20D0 00 E7 2A 01 E7 5D 01 E7 81 01 E7 B3 01 E7 0A 02
20E0 E7 94 02 E7 B4 02 E7 E0 02 E7 EF 02 C6 23 1C 05
20F0 20 D7 F9 F0 B2 23 1C C6 1F 1C 05 20 D7 F6 F0 B2
2100 23 1C 9A 1F 1C D7 06 05 20 D7 F4 F8 F0 F9 F0 99
2110 41 1C D3 11 99 5A 1C D1 0A 99 61 1C D3 07 99 7A
2120 1C D9 02 F8 F0 F9 F0 FA 36 15 05 FB FD FD 27 F7
2130 F0 C7 22 08 00 C7 22 09 1C A2 22 1C C3 22 04 1C
2140 C3 22 06 1C F0 A3 22 04 1E 8B 22 06 1E D7 06 9B
2150 22 08 00 D7 13 C8 20 B1 FF 20 C7 22 08 20 28 46
2160 C3 22 04 20 CC 20 F8 F0 F9 F0 A3 22 06 1E 8B 22
2170 04 1E D7 06 9B 22 08 00 DF 02 F8 00 F9 F0 A3 22
2180 06 1E 8B 22 04 1E D7 06 9B 22 08 00 DF 16 C8 20
2190 28 14 8B 22 04 20 D7 04 C7 22 08 00 C3 22 06 20
21A0 CC 20 F8 F0 F9 F0 BF 22 09 20 64 1E 20 8B 22 02
21B0 20 D3 03 A2 22 20 F0 C8 20 C8 1E C8 24 01 1C A3
21C0 22 02 20 6A 22 20 A3 22 04 1E 6B 22 06 1E A3 22
21D0 04 24 8B 22 06 24 D7 0B 9B 22 08 00 DF 16 A0 20
21E0 1C 20 08 D9 03 A0 20 1C 64 1E 1C 01 1E BF 22 09
21F0 20 8C 20 1C 88 00 1C CC 24 CC 1E CC 20 F0 F2 C7
2200 01 27 B1 1C A1 00 B0 1C A1 04 00 1E 8C 20 1C C0
2210 56 1C 4D 33 01 22 1C C0 58 1C 01 54 A1 2A 81 22
2220 C2 22 24 C3 22 02 26 B1 02 1C 2F 05 71 F8 48 B1
2230 20 1C 20 1A F2 C7 01 29 81 1C A1 00 B0 1C A1 04
2240 00 1E 8C 20 1C C0 5E 1C 71 7F 48 B1 21 1C 3E 15
2250 FD B0 1C 06 45 05 00 0A 04 F3 F0 F2 C7 01 28 81
2260 1C A1 00 B0 1C A1 04 00 1E 8C 20 1C C0 50 1C 11
2270 49 C7 01 26 81 00 71 7F 33 B0 33 16 A1 34 B1 22
2280 C2 22 24 C3 22 02 26 B1 02 1C 2E A5 2A 03 F3 F0
2290 C8 1C C8 20 C8 22 C8 1E B1 0C 1F 7B 01 27 81 1F
22A0 A1 00 E0 20 A1 FF FF 22 08 1F 20 09 01 1C 80 20
22B0 1C 08 1F 22 60 22 1C F9 3F 43 25 A1 2A B1 22 FA
22C0 2E 83 D3 05 FB FD FD 27 EE C2 1E 1C 3A 48 11 2E
22D0 56 45 19 00 0A 52 B1 30 06 A0 52 04 91 06 48 F8
22E0 FB CC 1E CC 22 CC 20 CC 1C F0 C8 1C C8 22 C8 1E
22F0 B1 FF 20 B3 01 02 40 21 39 21 72 B1 0C 1F 7B 01
2300 29 B1 1F A1 00 E0 20 A1 FF FF 22 08 1F 20 09 01
2310 1C B0 20 1C 08 1F 22 40 22 1C 5C B0 48 1C 32 1C
2320 03 39 1C F7 91 80 48 B0 48 1C 32 1C 05 39 1C 02
2330 27 F5 2D F3 45 14 00 0A 5A 08 01 5C DF 29 B1 21
2340 1C DB 03 B1 01 1C B0 1C 06 A0 5A 04 FD FD FD B1
2350 0B 06 A0 5A 04 64 5E 5A FB FD FD 90 16 31 FA 33
2360 31 F6 71 F7 31 27 D2 11 20 71 7F 48 FB 98 00 20
2370 CC 1E CC 22 CC 1C F0 C8 22 C8 1E 28 06 FB CC 1E
2380 CC 22 F0 A1 34 81 22 B1 FF 20 FA 3D 49 08 13 20
2390 2D D8 D3 02 11 20 98 00 20 F0 C8 22 C8 1E F9 3F
23A0 43 21 FB FD FD 2F DC DF F5 71 80 20 2D D0 A2 1E
23B0 1C 37 1D 06 91 01 20 71 7F 1D 98 00 20 F2 71 DF
23C0 49 F3 F8 FB CC 1E CC 22 F0 99 13 1C DF 09 99 11
23D0 1C D7 07 71 FE 48 F0 91 01 48 F0 01 22 3B 06 06
23E0 05 22 D7 F9 20 4B B1 05 1C 01 22 A0 0A 1E 33 06
23F0 0A 05 22 D7 F6 15 1C D7 F0 20 36 A0 0A 22 33 06
2400 FA 48 1E 22 1C A0 1C 20 B1 14 22 E0 22 FD 05 20
2410 D7 F6 A1 6E 00 20 89 2E 0E 1C D9 15 A1 80 01 22
2420 A1 B0 04 20 8B 22 1C D1 08 09 01 22 08 01 20 27
2430 F3 F0 32 48 5A B1 24 08 F8 39 48 1D 64 56 52 08
2440 01 54 DF 12 B1 10 44 D3 03 B1 30 44 2C D9 B0 44
2450 06 A0 52 04 F3 F0 91 02 48 44 58 0A 52 3F 48 E9
2460 38 48 E6 B3 01 02 40 44 3B 44 DE C8 1E A0 22 44
2470 A1 2A 81 22 2D 08 A0 44 22 DB 0F A2 1E 54 CC 1E
2480 71 FD 48 45 14 00 0A 52 27 BF CC 1E 71 F9 48 F3
2490 F0 B1 A0 15 71 F3 34 91 08 34 B0 34 03 91 04 32
24A0 B0 32 15 F0 32 35 1C 71 F8 32 B0 32 15 44 50 50
24B0 46 64 50 46 08 03 46 44 46 36 4C 2C 6A B1 1A 06
24C0 A0 4C 04 F3 F0 B0 06 46 71 F8 31 B1 08 08 F8 3C
24D0 49 0E 3B 46 23 01 4A A1 01 00 4E 91 10 49 20 82
24E0 51 0F 49 47 9B 01 28 81 47 DF 10 33 46 03 80 4E
24F0 4A 09 01 4E 17 49 20 6A 2F 97 F0 3B 46 03 91 80
2500 4B A0 22 46 C8 1E A1 34 81 22 2C 39 D3 05 91 20
2510 49 20 03 C2 1E 4A CC 1E A0 46 22 71 E0 49 2F 71
2520 99 20 4A DB 3C 11 46 99 11 4A D7 03 91 02 46 99
2530 13 4A D7 03 91 01 46 99 03 4A D7 03 91 80 46 99
2540 1B 4A D7 03 91 40 46 99 01 4A D7 03 91 20 46 99
2550 06 4A D7 03 91 10 46 93 01 26 B1 46 C7 01 26 B1
2560 46 F0 64 50 4C EF BF FB B1 1A 06 A0 4C 04 F0 FA
2570 A1 00 86 18 B0 00 09 3E 15 FD B1 20 06 45 05 00
2580 0A 04 FD 3E 15 FD B1 21 06 45 05 00 0A 04 01 1C
2590 05 1C D7 FC 11 43 B1 20 33 B0 33 16 B1 A0 32 B0
25A0 32 15 B1 02 0E B1 80 0E B1 09 11 C4 00 07 B1 20
25B0 30 11 31 11 34 B0 34 03 B1 93 1C C7 01 03 40 1C
25C0 B1 1F 1C C7 01 02 40 1C A1 80 2D 22 A1 00 80 1E
25D0 A1 12 00 20 EF 1D FB A1 D4 26 1C C3 01 56 80 1C
25E0 A1 D6 26 1C C3 01 58 80 1C A1 D4 26 1C C3 01 5A
25F0 80 1C A1 D4 26 1C C3 01 5C 80 1C A1 00 88 1C C3
2600 01 42 80 1C A1 2C 02 1C C3 01 44 80 1C A1 6F 25
2610 1C C3 01 40 80 1C C3 01 52 80 00 A1 B0 04 20 EF
2620 B9 FD C8 20 B1 08 1C A1 3C 00 22 A1 5E 80 24 A1
2630 C2 80 26 EF C8 FB CC 20 B1 08 1C A1 C2 80 24 A1
2640 26 81 26 EF 15 FC B1 08 1C A1 C0 12 20 EF E4 FB
2650 A1 A1 2C 22 A1 00 86 18 B1 2C 08 FB 20 04 A1 C8
2660 2C 22 2A 87 2A 99 DB 1F A1 52 2D 22 9A 22 00 DF
2670 16 9A 22 1C DF 06 65 04 00 22 27 F0 C9 85 26 CB
2680 22 02 29 8B F0 D3 D7 11 43 A1 CC 2C 22 27 D3 32
2690 31 03 EF 30 FE FA B3 01 26 81 41 31 41 03 71 FE
26A0 48 30 41 03 91 01 48 C7 01 26 81 00 71 F0 41 DF
26B0 23 90 41 43 36 43 05 CB 01 58 80 F0 37 43 05 CB
26C0 01 56 80 F0 35 43 05 CB 01 5A 80 F0 34 43 05 CB
26D0 01 5C 80 F0 F3 F0 31 43 FB CF 01 44 80 C3 01 4C
26E0 80 22 CC 22 20 0D CF 01 44 80 C3 01 4C 80 22 CC
26F0 22 05 22 C3 01 46 80 1C C3 01 4A 80 20 C3 01 48
2700 80 1E C3 01 40 80 22 C3 01 4E 80 24 C3 01 50 80
2710 26 C3 01 42 80 18 8B 01 52 80 22 D7 0D B3 01 54
2720 80 1C C6 22 1C C3 01 52 80 00 11 43 B1 11 1C EF
2730 97 FC A1 36 2D 22 29 B3 A3 01 40 80 22 29 8E A1
2740 44 2D 22 29 A6 A3 01 44 80 22 29 81 A1 4B 2D 22
2750 29 99 A3 01 42 80 22 29 74 A1 C8 2C 22 26 F5 F2
2760 CB 01 00 80 F0 F2 CB 01 02 80 F0 F2 B0 06 35 A0
2770 04 36 CB 01 04 80 F0 F2 CB 01 06 80 F0 F2 CB 01
2780 08 80 F0 F2 90 16 31 CB 01 0A 80 F0 F2 CB 01 0C
2790 80 F0 F2 CB 01 0E 80 F0 F2 CB 01 10 80 F0 29 3C
27A0 DB 6C B1 3A 1C 29 B2 DB 65 11 21 B0 20 1C 28 19
27B0 DB 5C B0 23 1C 28 12 DB 55 B0 22 1C 28 0B DB 4E
27C0 11 1C 98 00 20 D7 02 17 1C 74 1C 21 C8 1C 18 04
27D0 1C 28 04 CC 1C DB 37 71 0F 1C 99 09 1C D1 03 75
27E0 07 1C 75 30 1C 21 72 11 20 2F B3 58 21 00 1C 27
27F0 D8 29 26 DB 19 28 3D DB 15 19 04 1C B0 1C 1D 29
2800 18 DB 0B 28 2F DB 07 90 1D 1C 74 1C 21 F8 F0 C8
2810 1C B1 20 1C 29 43 CC 1C F0 28 FE DB 16 C8 20 B0
2820 1C 20 28 10 DB 0B B0 1C 21 B0 20 1C 29 2B B0 21
2830 1C CC 20 F0 99 30 1C D3 17 99 39 1C D1 0D 99 41
2840 1C D3 0D 99 46 1C D9 08 79 07 1C 79 30 1C F8 F0
2850 F9 F0 C8 22 28 19 DB 14 99 20 1C DF 0B 99 2C 1C
2860 DF 06 F9 99 0D 1C D7 04 B0 22 1D F8 CC 22 F0 01
2870 22 2F A6 DB 0B 09 04 22 74 1C 22 27 F4 99 08 1C
2880 D7 0C 08 04 22 B1 5C 1C 2B CF DB 15 27 E3 99 0D
2890 1C DF 0C 99 2C 1C DF 05 99 20 1C D7 04 2B BA F8
28A0 F0 F9 F0 C8 1C 18 04 1C 28 04 CC 1C DB 14 C8 1C
28B0 71 0F 1C 99 0A 1C D3 03 75 07 1C 75 30 1C 28 99
28C0 CC 1C F0 2F AA DB 05 A0 22 20 2F A3 F0 C8 1C B0
28D0 23 1C 2F CF B0 22 1C 2F CA CC 1C F0 C8 1C B1 0D
28E0 1C 28 76 B1 0A 1C 28 71 CC 1C F0 C8 1C B2 23 1C
28F0 98 00 1C F8 DF 06 28 61 DB 02 27 F1 CC 1C F0 28
2900 18 DB 15 C8 1C 11 1D 99 0D 1C D7 08 28 5C DB 06
2910 A1 0A 00 1C 28 54 CC 1C F0 C8 1E C8 22 C8 20 B0
2920 1D 40 3F 43 27 EF 72 FA DB 22 99 11 1C DF F3 99
2930 13 1C DF EE 99 03 1C DF E9 99 1B 1C DF E4 99 01
2940 1C DF DF 99 06 1C DF DA F8 37 43 03 11 1C F9 B0
2950 40 1D CC 20 CC 22 CC 1E F0 C8 1C 11 1D 30 43 05
2960 28 20 CC 1C F0 28 03 CC 1C F0 C8 1E C8 22 C8 20
2970 C8 1C F9 3F 43 03 EF 17 F9 CC 1C CC 20 CC 22 CC
2980 1E F0 C8 20 F9 3F 43 06 EF 5F F9 D7 F7 F8 CC 20
2990 F0 B1 08 1C C7 01 03 40 1C B1 28 1D E0 1D FD 95
29A0 01 1C 05 20 D7 EE 91 01 1C C7 01 03 40 1C F0 28
29B0 21 E3 1E 28 1D C8 20 C9 BC 29 E3 1E CC 20 B0 20
```

```
29C0 21 28 0F F0 28 0C B2 1E 1C 27 F3 28 05 C6 1E 1C
29D0 27 EC CC 22 71 C0 21 B3 01 02 40 20 B0 20 1D 71
29E0 3F 1D 90 21 1D C7 01 02 40 1D 71 C0 20 E3 22 2E
29F0 7E DB 42 2E E7 2E D6 2E 16 28 3C B2 1E 1C 2E A3
2A00 2E 0D 2E 4E DB 11 C6 1E 1D 9A 1E 1D DF 05 B1 3F
2A10 1C 2F 46 07 22 27 DC 2F 40 DB 1A 99 2F 1C DF F3
2A20 99 2D 1C D7 04 05 22 27 EC 99 40 1C DF C1 99 3D
2A30 1C DF BC F8 F0 F9 F0 A0 22 1E B9 28 00 22 DB 1B
2A40 B9 18 00 22 D3 15 B9 1A 00 22 DF 0F B9 1B 00 22
2A50 DF 09 49 1B 00 22 1E 65 42 80 1E F0 2E 11 DB 62
2A60 A0 22 1E 88 00 1E D7 05 A3 01 40 80 1E 99 0D 1C
2A70 DF 1C 2D FB DB 4C 99 0D 1C D7 47 B2 22 1C C7 01
2A80 54 80 1C C3 01 52 80 22 B1 F7 1C C6 22 1C 2E 4C
2A90 3A 48 FD FA 91 02 43 A3 01 42 80 18 CB 1E A3 01
2AA0 46 80 1C A3 01 4A 80 20 A3 01 4C 80 22 A3 01 48
2AB0 80 1E A3 01 4E 80 24 A3 01 50 80 26 CB 01 44 80
2AC0 F3 F0 F9 F0 A1 12 2D 22 B1 FF 1F 20 06 A1 EC 2C
2AD0 22 11 1F 11 1E 2E 14 DB 73 91 04 43 2E 3B DB 7F
2AE0 99 3A 1C D7 F7 11 21 2D 08 DB 61 B0 1C 20 2D 01
2AF0 DB 5A B0 1C 23 2C FA DB 53 B0 1C 22 2C F3 DB 4C
2B00 99 01 1C DF 4C 99 00 1C D7 2A 2C E5 DB 26 C8 1E
2B10 2F 25 A0 1E 24 CC 1E 98 00 1F D7 03 C6 24 1C 9A
2B20 24 1C D7 10 07 22 E0 20 E1 2C C6 DB 1F 98 00 21
2B30 D7 02 27 A8 B1 FF 1E 71 FB 43 C8 22 A1 FE 2C 22
2B40 2D A9 CC 22 DB 06 2D 85 DB 02 27 8D 71 FB 43 F9
2B50 F0 2C 9E DB F7 98 00 21 D7 DA C3 01 40 80 22 98
2B60 00 1E D7 E8 71 7B 43 A1 D1 2C 22 2D 7E A3 01 40
2B70 80 22 2D 59 F8 F0 2D 4B DB 5B A0 22 1E 01 24 99
2B80 0D 1C DF 07 2C E9 DB 4D A0 22 24 68 20 1E 07 1E
2B90 A0 20 22 91 04 43 88 00 1E DF 2D B1 10 20 89 10
2BA0 00 1E DB 03 B0 1E 20 EF F4 FB DB 29 C8 1E 2E 87
```

```
2BB0 B2 1E 1C 07 22 CC 1E EF 0F FC DB 19 05 1E E0 20
2BC0 EB EF 27 FC DB 0F 27 CE A0 24 22 88 00 22 DF 02
2BD0 2C 15 2D 08 F8 F2 71 FB 43 F3 F0 2C E6 DB 57 91
2BE0 01 43 A1 10 00 24 28 0E 2C F2 71 FE 43 F0 2C D3
2BF0 DB 44 A1 08 00 24 48 20 22 1E 07 1E A0 20 22 88
2C00 00 1E DF 31 B0 24 20 88 24 1E DB 03 B0 1E 20 2C
2C10 CB DB 23 2C B8 DB 1F EF F5 FB C8 1E 2E 19 B2 1E
2C20 1C 07 22 CC 1E 2C 7C DB 0D EF E3 FB DB 08 05 1E
2C30 E0 20 E7 27 CA F8 F0 A1 26 2D 22 2C AE 2C DA DB
2C40 0B 99 59 1C DF 07 99 4E 1C D7 F2 F8 F0 FF 27 FE
2C50 2C 1D 98 00 22 D7 26 99 03 23 D3 21 99 48 23 D9
2C60 1C B0 23 22 18 04 22 5D 0A 22 20 71 0F 23 74 20
2C70 23 5D 64 23 20 B1 08 1C EF B9 F5 F8 F0 F9 F0 2C
2C80 7E D3 FC F8 F0 EF CA FB DB 15 99 01 1D D9 10 B1
2C90 0E 1C 30 1D 03 B1 0F 1C C7 01 03 40 1C F8 F0 F9
2CA0 F0 0D 0A 0D 0A 38 30 39 38 20 4D 6F 6E 69 74 6F
2CB0 72 20 56 31 2E 38 20 62 79 20 4A 2E 4D 2E 20 57
2CC0 61 6C 64 20 31 39 38 39 0D 0A 3E 00 3F 0D 0A 3E
2CD0 00 0D 0A 46 69 6C 65 20 72 65 63 65 69 76 65 64
2CE0 20 4F 6B 0D 0A 45 78 65 63 3A 20 00 0D 0A 4C 6F
2CF0 61 64 69 6E 67 20 66 69 6C 65 2E 2E 2E 00 0D 0A
2D00 45 72 72 6F 72 20 69 6E 20 66 69 6C 65 20 61 74
2D10 20 00 0D 0A 56 65 72 69 66 79 69 6E 67 20 66 69
2D20 6C 65 2E 2E 2E 00 0D 0A 52 65 73 65 74 3F 20 28
2D30 59 2F 4E 29 20 00 0D 0A 42 72 65 61 6B 21 20 50
2D40 43 3A 20 00 20 50 53 57 3A 20 00 20 53 50 3A 20
2D50 00 FF 43 00 85 2C 53 00 EF 29 47 00 5C 2A 4C 00
2D60 CD 2A 50 00 76 2B 44 00 EE 2B 52 00 37 2C 54 00
2D70 DB 2B 42 00 50 2C 45 00 7F 2C 56 00 C4 2A 00 FF
2D80 D4 26 D4 26 A4 24 32 24 D4 26 8F 26 D4 26 D4 26
2D90 E6 26
```

DESKTOP WEATHER PICTURES

Weather pictures can be brought direct from a satellite to a desk top computer with the 'Dartcom System'. Developed by British Aerospace in collaboration with the Dartcom Partnership, the system, which costs less than £5,000, can receive automatic picture transmission (APT) images from any current met satellite and then store, process or display the pictures on a PC. The geostationary and polar orbiting satellites it can tap include GOES, METEOSAT, NOAA, METEOR, COSMOS and OKEAN. The system can also display certain high resolution archive images such as those from the US Landsat and French Spot satellites.

ELECTRONICS SCENE

With the aid of infra-red techniques, the routes will be transmitted to an in-vehicle unit in subscribers' vehicles that will provide simple instructions to the driver on the best route to follow. The system indicates to drivers where to turn and which lane to use.

AUTOGUIDE SYSTEM WILL SPEED LONDON TRAFFIC

By the end of 1993, all London drivers will have access to the new GEC 'Autoguide'vehicle guidance system that promises to cut journey times and driver fatigue. A pilot scheme will be operational in central London by 1992 and will be expanded progressively to become generally available a year later.

'Autoguide' will provide the driver with up-to-the-minute directions for the best route to a chosen destination, allowing a significant reduction in journey times within London's M25 motorway ringroad.

The heart of the system is a central computer that collects journey times from roads in and around the capital. The preferred routes are continuously updated and broadcast to subscriber vehicles from a network of strategically located roadside beacons.

HIGH-SPEED BUFFERS IMPROVE SATELLITE COMMUNICATIONS

High-speed Doppler plesiochronous buffer system, working at rates of up to 36 Mbit/s have been developed by Cybermation. The first system has already been supplied to ANT Nachrichtentechnik for use on satellite links into Berlin.

Plesiochronous buffers are used at satellite ground stations to remove timing impairments, correct jitter and prevent timing slips caused by satellite movement and differing reference clocks. Now that satellites are being allowed a larger North / South axis drift to save fuel and to extend working life, the timing and Doppler problems are becoming more acute.
(Ed. note: two or more signals are said to be plesiochronous if their corresponding significant instants occur at the same **rate** but not in the same **phase**).

DIGITAL STEREO SOUND ON ITV TRANSMISSIONS

Independent Television (ITV) transmitters covering the London area (Crystal Palace) and a large part of Yorkshire (Emley Moor) became fully operational for digital stereo sound in September.

The new sound system, known as NICAM 728, has been developed jointly by broadcasters and receiver manufacturers. It may be used to enhance a wide variety of different types of programme, adding a new and worthwhile dimension of realism to the small screen.

To take advantage of the stereo sound, it is necessary to use a television receiver or video recorder equipped for NICAM.

The Independent Broadcasting Authority intends to extend the availability of NICAM transmissions to reach about 75% of the UK population by the end of next year.

MAGAZINE FOR VINTAGE-RADIO ENTHUSIASTS

A new bi-monthly magazine for vintage-radio enthusiasts, *RADIO BYGONES*, has been published recently by G.C. Arnold Partners. It covers domestic radio and TV, amateur radio, commercial systems both fixed and mobile, and military, aviation and marine communications, from the days of Hertz, Maxwell and Marconi to what was state-of-the-art only a few years ago.

Editorial features will include articles on restoration and repair, history, reminiscences and just plain nostalgia, plus features on museums and private collections.

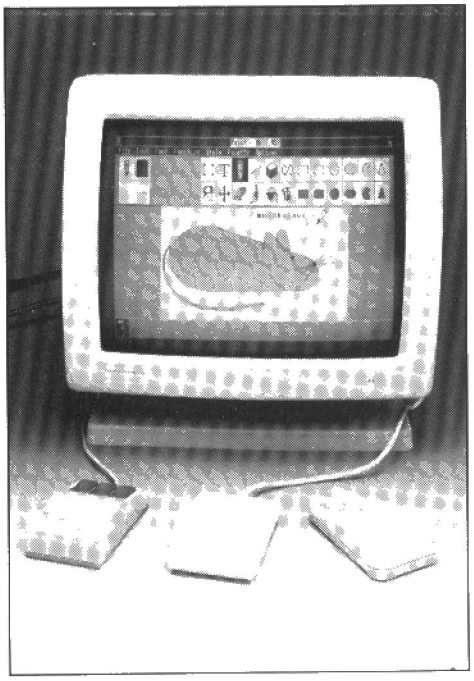
Publisher and editor of the magazine is Geoff Arnold, who first became interested in radio during the Second World War, and spent over twenty years in professional radio and electronics before becoming a journalist. He has been involved in publishing since 1973 and has been editor of *PRACTICAL WIRELESS* for 12 years.

COMPUTER MOUSE

J. Ruffell

Raptly looking at the screen and cheerfully moving the mouse around on our desks to make our way through menus, few of us appear to be aware of the operation of the most popular pointing device for computer applications.

A computer mouse is also called a *pointing device* because it allows the cursor (usually an arrow or crosshairs) to be moved across the computer screen. You use your hand to control the direction and speed of the cursor. Many mouse-oriented programs allow you to select an option from a menu on the screen simply by pointing at it and clicking a button on the mouse. The mouse has become so popular because it obviates keyboard commands that distract the attention from the screen and are relatively slow and susceptible to errors. Another major application of the computer, drawing, would be unthinkable without a mouse.



Principle of operation

One aspect common to all computer mice is that movement is converted into signals that can be handled by a computer. This is achieved basically as shown in Fig. 1. An auxiliary spindle presses a small ball lightly against two spindles that are mounted at right angles to each other. Its own weight, and in some cases the auxiliary spindle also, keeps the ball in contact with the desk surface or mouse pad. The movement of the ball is hardly obstructed because the areas where the spindles touch the ball are small. The friction is, however, sufficient to cause the spindles to rotate if the ball is moved horizontally (x component) or vertically (y component) in a two-dimensional plane. In this manner, the spindles extract the horizontal and vertical components from the mouse movement. These two components are converted into four electrical signals. This is done by mounting a slotted disk on to each spindle. The slots are arranged such that the light beam of one optocoupler is fully passed when the other optocoupler is about half way open. As the spindle rotates, the optocouplers produce two rectangular signals with a phase difference of 90°. The direction of travel of the spindle (in one plane) can be deduced from the phase relation of the two signals. The number of periods of the rectangular signal indicates the relative distance covered by the ball, and its speed.

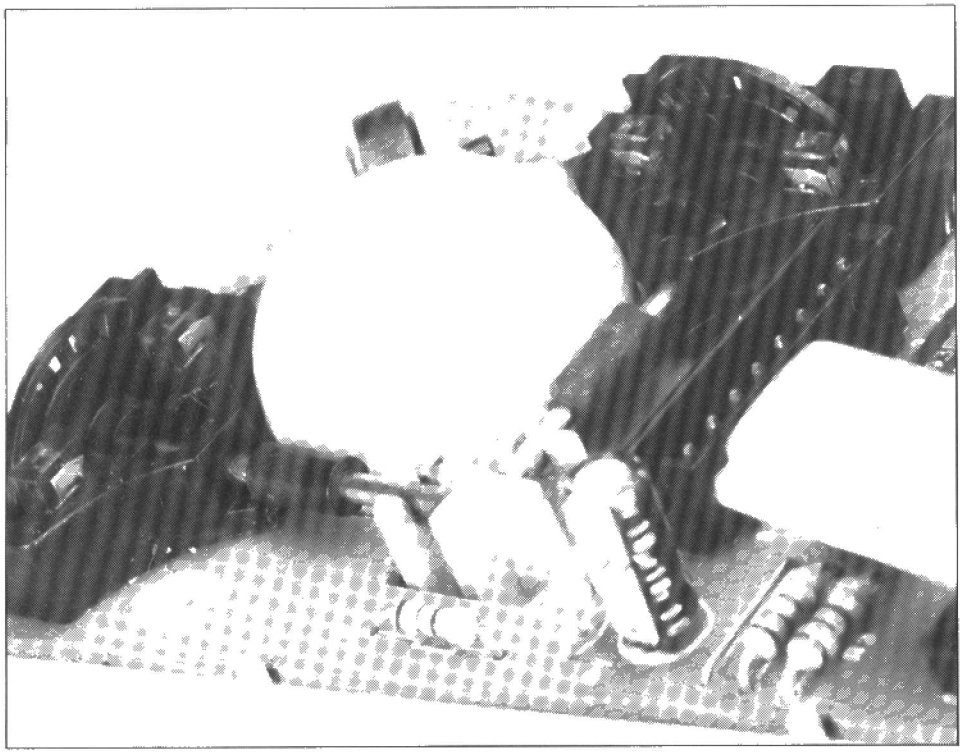


Fig. 1. Basic construction of a mouse that converts ball movement into electrical signals.

Figure 3 shows how the two rectangular signals are used to deduce the direction of travel of the mouse. One optocoupler signal is called *reference*, the other *direction*. The reference signal determines the instant the minimum step size (distance travelled) is reached in the direction indicated by the direction signal. This instant is marked by one of the level transitions (pulse edges) of the reference signal. Since most computer interrupts are called by negative pulse edges, it is convenient to look at the 1-to-0 transition of the reference signal. As shown in Fig. 3a, the direction signal is logic high at the negative edge of the reference signal. For the opposite direction, however (Fig. 3b), the direction signal is low at the negative edge of reference signal. In terms of programming, this means that the number representing the cursor position on the screen must be changed on the falling edge of the reference signal. In this software routine, the direction signal must be read to determine whether the cursor position must be incremented or decremented at a particular step size, e.g., one screen position. If, after first connecting a mouse and installing the software

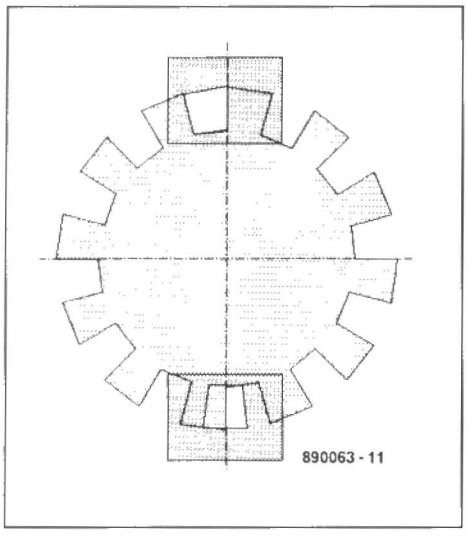


Fig. 2. Slotted discs and optocouplers are used to digitise ball movement.

driver, the cursor movement is opposite to that of the mouse, the reference and direction signals probably need to be swapped.

The above description of the basic operation of a mouse applies, at least in principle, to most other pointing devices that allow the user to control the cursor position on the screen direct by moving the mouse accordingly. There are, however, also applications that require a different approach. Take, for instance, a program that enables a drawing on paper to be copied into the computer by means of a mouse. In this case it is the drawing, not the computer screen, that determines the cursor position. This type of mouse is known as a *digitiser*, and is usually supplied with a special pad. The paper is inserted between the digitiser and the pad. The window in the digitiser 'sees' the pad surface through the paper. Because the pad 'communicates' with the digitiser, an output signal is available that enables the computer to determine the absolute position above the pad, and, of course, above the paper, which is secured on it. Lifting the digitiser and putting it down again a little further is therefore perfectly acceptable, since the new position is detected immediately. This is in contrast with a ball-type mouse, which can not supply positional information if it is lifted from the desk.

Another system to convey positional information to the computer is a combination of a graticule pad and a mouse with built-in reflection sensors. The internal operation is functionally similar to that of the discs and spindles in the ball-type mouse. The optocouplers are replaced by sensors that detect the light reflected by the pad. The function of the discs is taken over by the pad with its pattern of light and dark areas. Like the ball-type mouse, the optical mouse produces a reference and a direction signal. Its clear advantage is, of course, the absence of moving parts. However, the optical mouse also has its disadvantages: these are mainly that the pad has to be kept clean, and that the pattern on it is critical.

To the computer

The simplest way to convey the rectangular output signals supplied by the mouse is, of course, by means of a cable. The computer has either a built-in mouse adapter ('bus mouse', e.g. the Amstrad PC1512/1640 series), or a standard RS232 serial port to which a mouse with built-in 'intelligence' can be connected (e.g., most standard IBM PCs and compatibles). The latter mice are often microcontroller-driven, and supplied with a special software program, called the mouse driver, that enables the PC to translate data received at high speed via the RS232 port to be translated into cursor movement. The current required for powering the circuit in the RS232 mouse is obtained from the computer's serial port. This is possible only by virtue of the low current drain of the serial mouse.

The latest in pointing device technology is the wireless mouse, which communicates with the computer via an infra-red link. Position output and the way the data is processing in the driver are, however, not different from those of the conventional 'mouse with tail'.

Signal processing

As already stated, the mouse signals are usually processed by means of a driver program installed on the computer. Most computer users will content themselves with being able to automatically install the mouse with the correct parameters as part of the system configuration programs called at power-on. For advanced applications, however, mouse manufacturers like Genius supply a programming guide and auxiliary programs (e.g., Genius Menu Maker) that give the user the opportunity to implement his own pull-down menus and mouse control in a particular program.

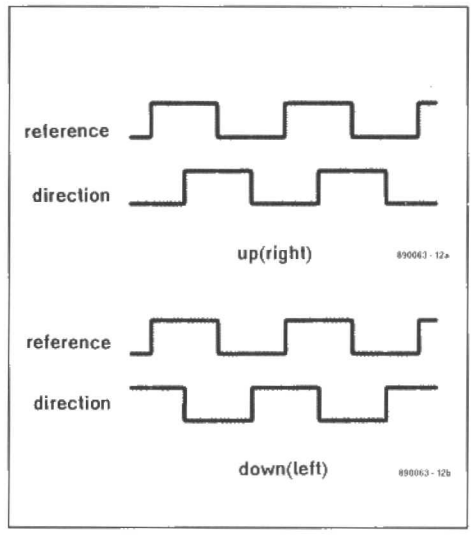


Fig. 3. The phase relation between the reference and direction signals is used to deduce the direction of travel.

Among the many functions of the driver or the microcontroller in the serial mouse is *adaptive resolution control*, or control of the step size as a function of mouse speed. If the mouse speed exceeds a certain predefined value, the cursor step size is automatically increased. The advantage of this system is that a relatively small mouse movement enables large distances to be covered rapidly on the screen.

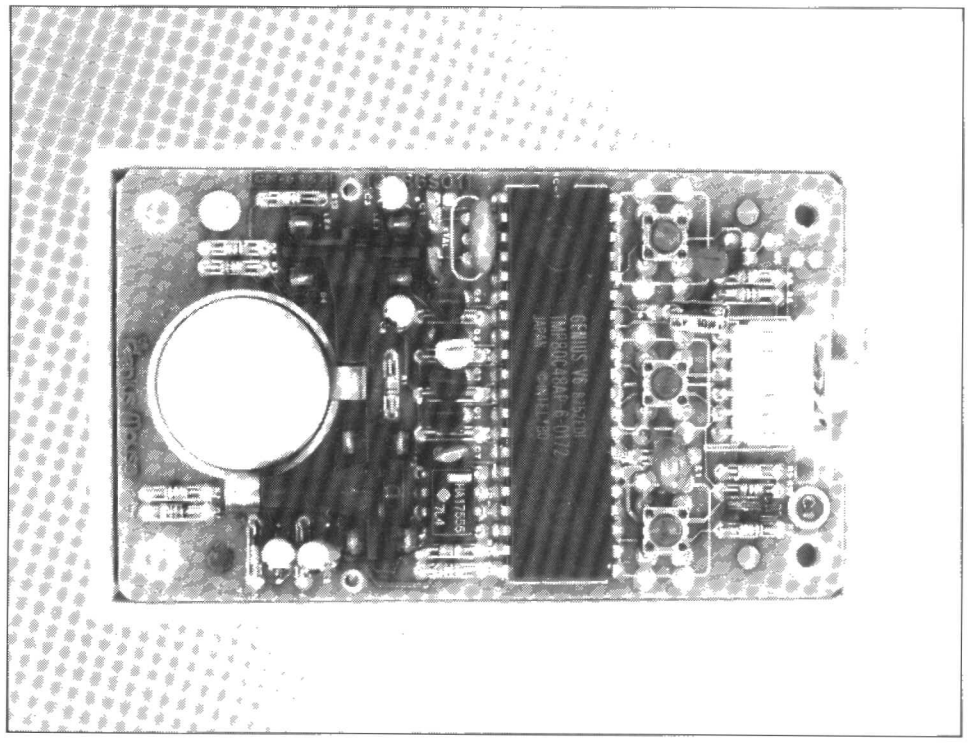


Fig. 4. Serial mouse with on-board CMOS microcontroller to guarantee a low current drain from the RS-232 port on the computer.

APPLICATION NOTES

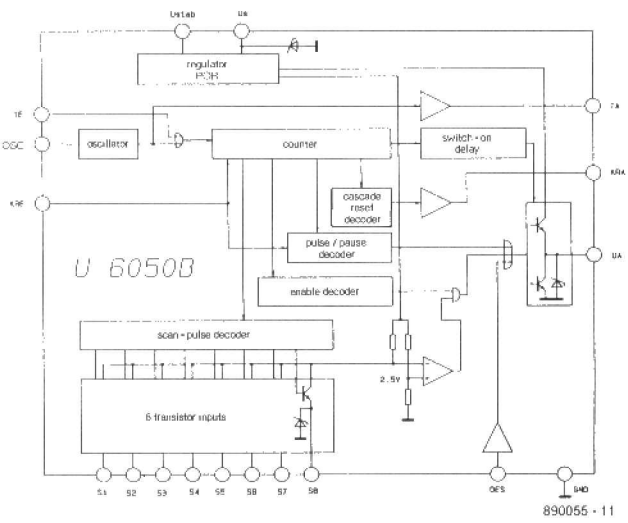
The contents of this article are based on information obtained from manufacturers in the electronics industry, and do not imply practical experience by *Elektor Electronics* or its consultants.

MULTIPLEX CONTROL WITH U6050B/6052B

Automotive and industrial electronics often require a number of actuator data or control commands to be conveyed simultaneously. Traditionally, the feedback data for each process is sent over a dedicated wire or pair of wires. Telefunken Electronic GmbH of Federal Germany have recently launched the U6050 family of integrated circuits that allow multiple commands or data to be sent over a single wire or pair of wires.

Telefunken's Type U6050B (transmitter) and U6052B (receiver) chips are used for permanent scanning of 8 switch positions, serial data transmission via a single wire, and subsequent control of 8 relays.

A so-called master-slave cascade of two transmitters and two receivers allows 16 input signals to control an equal number of outputs. Data purity between the transmitter and the receiver is ensured by quadruple comparison. When the receiver detects interference, it automatically disables its outputs to avoid erroneous control of output de-



Pin	Function
S1 – S8	switch inputs 1 – 8
Us	supply voltage
Ustab	5.2 V regulated
OSZ	R-C oscillator input
TE	clock input for cascade
DA	data output
TA	clock output for cascade
KRE	cascade reset input
KRA	cascade reset output
DES	data input slave
GND	ground

Fig. 1. Block diagram of the multiplex transmitter Type U6050B.

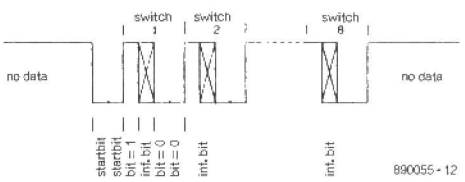


Fig. 2. Bit functions in the serial dataword.

Start pulse:	312 µs
'One' bit:	156 µs
Information bit:	156 µs
'Zero' bit	156 µs
Infomation block:	625 µs
Dataword:	5 ms + 312 µs start bit
Data pause:	9.688 ms
Transfer cycle:	15 ms
Minimum response time:	60 ms
Dataword master-slave:	10 ms + 312 µs start bit
Data pause master-slave:	4.688 ms
Scan pulse:	312 µs
Switch-on delay:	75 ms

Table 1. Pulse timing at an oscillator frequency of 6.4 kHz.

vices. The relay output driver may be clocked to minimize dissipation.

The chips are housed in DIL-18 enclosures. Their specifications should meet the demanding requirements as regards the temperature range for automotive applications. The unregulated supply voltage range is 6 V to 16 V, but operation at 5 V is also possible with voltage regulation and a modified configuration of external components. The usable supply voltage range then becomes 4.3 V to 6.0 V.

Transmitter U6050B

The block diagram of transmitter chip Type U6050B is shown in Fig. 1. Like many electronic devices for automotive applications, the U6050B requires an external *R-C* network in the supply line to suppress noise. The resistor in this network also serves as the current limiter for the zener diode in the chip. The internal timing of both the transmitter and the receiver is controlled by an on-chip oscillator. The charge time, t_1, of this oscillator is determined by external resistor R_{OSZ}, and the discharge time, t_2, by an on-chip 2 kΩ resistor. Since the tolerance and temperature co-efficient of the internal resistor are greater than those of the external resistor, the ratio t_1/t_2 must be greater than 20 for all practical purposes. The minimum value of R_{OSC} is 68 kΩ.

The recommended frequencies for the transmitter and the receiver are 6.4 kHz and 25.6 kHz respectively. The resultant transmission parameters are listed in Table 1.

The U6050B scans its 8 input lines in a cyclic manner. For reliable key recognition a minimum current of 2 mA is required. Automotive applications require a current limiting 100 Ω resistor to be fitted in series with each input.

The voltage at the addressed input is compared with a reference potential of 2.5 V. An open switch is detected when the voltage is higher than the reference level. The IC detects a closed switch if the voltage is below the reference. The reference level adopted allows a contact resistance of up to 2.5 kΩ.

As shown in Fig. 2, the transmitter converts the current switch configura-

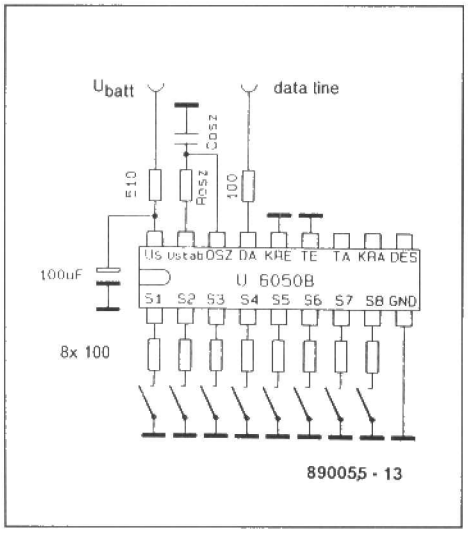


Fig. 3. Basic application diagram of the transmitter multiplexer.

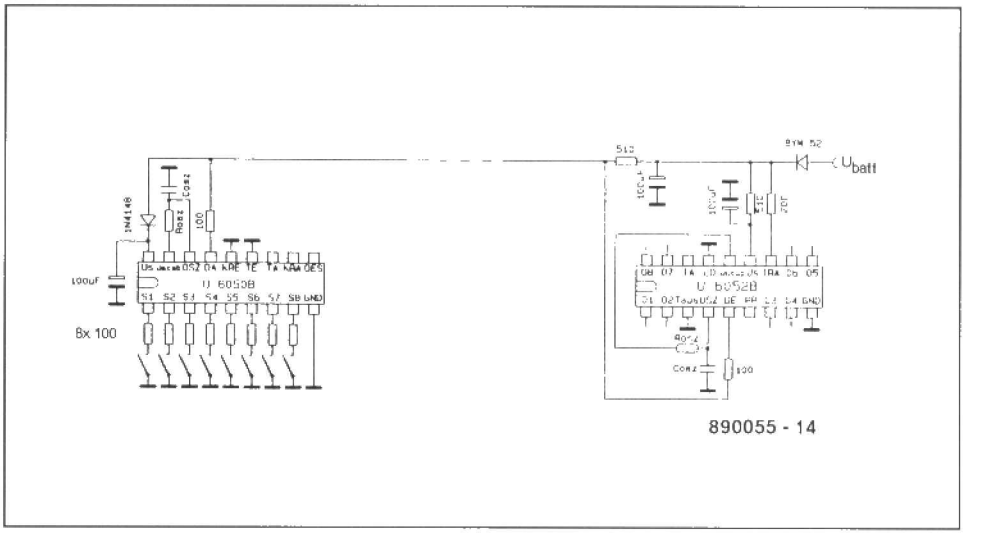
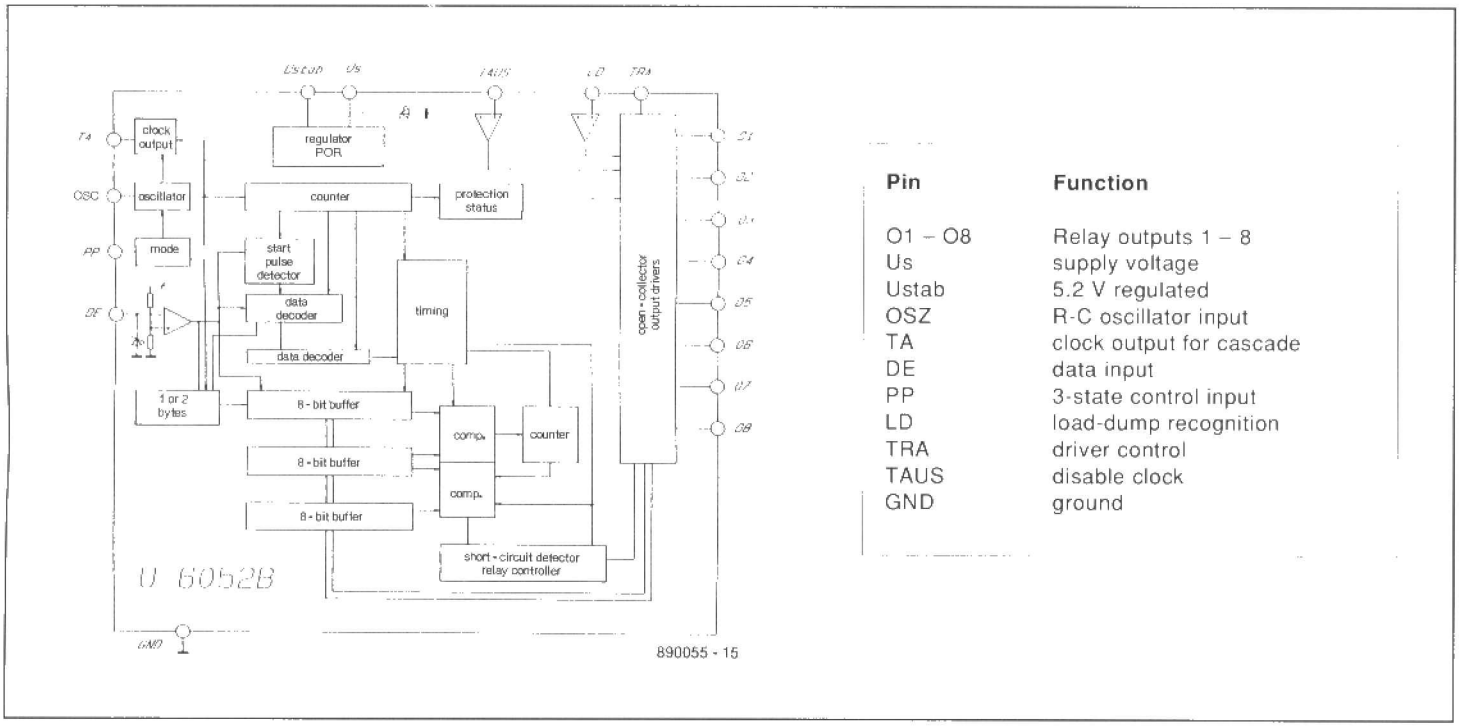


Fig. 4. The transmitter may also be powered via the serial dataline as shown here.



Pin	Function
O1 – O8	Relay outputs 1 – 8
Us	supply voltage
Ustab	5.2 V regulated
OSZ	R-C oscillator input
TA	clock output for cascade
DE	data input
PP	3-state control input
LD	load-dump recognition
TRA	driver control
TAUS	disable clock
GND	ground

Fig. 5. Internal structure of the receiver multiplexer Type U6052B.

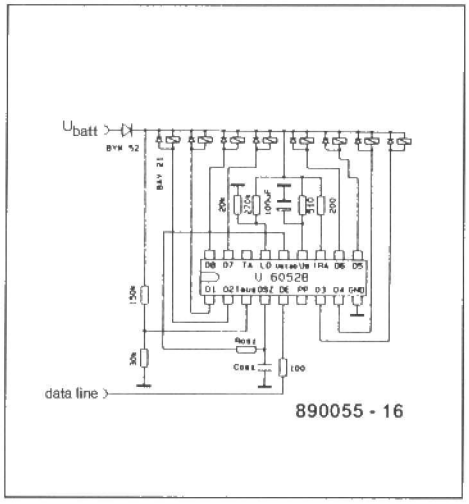
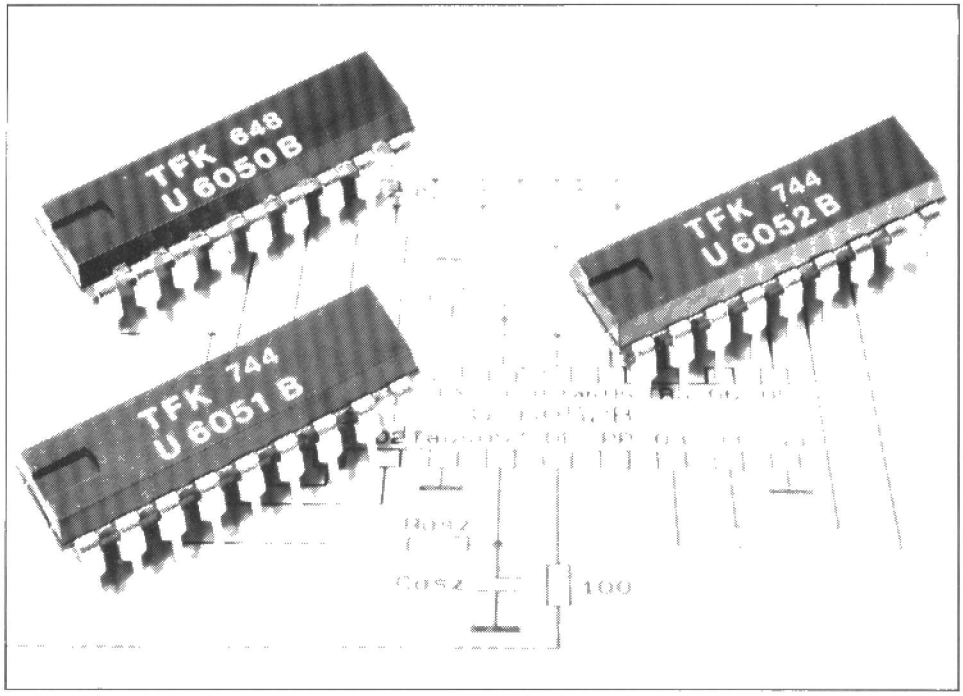


Fig. 6. Basic receiver application circuit with 8 relays.



tion at its inputs into a serial data word. Apart from the key identification data, the word contains a number of bits that serve to keep the transmitter and the receiver synchronized.

The switch information is composed of 4 parts:

- a '1' for receiver synchroniaztion
- an information bit ('1' = switch open; '0' switch = closed)
- a '0'
- a '0'

The dataword consists of 2 start bits and 8 information blocks. At a transmitter clock of 6.5 kHz, the length of the dataword is 5 ms plus the start bit, followed by a data pause (logic '1') of about 10 ms. This information is supplied repetitively as long as the transmitter is powered.

On power-up, the transmitter chip performs a reset operation that clears the internal logic circuits, and disables the data output for about 75 ms. This delay allows the buffer capacitor to be charged when the chip is powered via the dataline.

The transmitter output is of the push-pull type. A short-circuit of the output to the positive or negative supply line results in a current of only 30 mA. Voltage spikes are eliminated by an on-chip zener diode between pin DA and GND. The 100 Ω resistor shown in the application circuit of Fig. 3 limits the zener current to a safe value.

Receiver U6052B

The receiver decodes the dataword and checks its validity. On detection of a negative pulse transition at its input, the U6052B introduces a short delay to determine whether this is caused by a data pulse or interference. Too short pulses are treated as interference, and result in the receiver having to wait for the next transition. On detection of a start pulse, the chip loads the 8 successive bits into a receive register. In case fewer than 8 bits are received, for instance, as a result of interference or non-synchronized operation, the entire dataword is ignored. The receiver is synchronized by each '1' bit, and the logic level of any bit is established at about half way during the on-time.

The receiver operates at four times the transmitter clock frequency to allow the simple *R-C* timing networks to guarantee the reliability of the system, whose operation is consequently not degraded by frequency deviations of up to 15%.

Data purity is checked by comparing

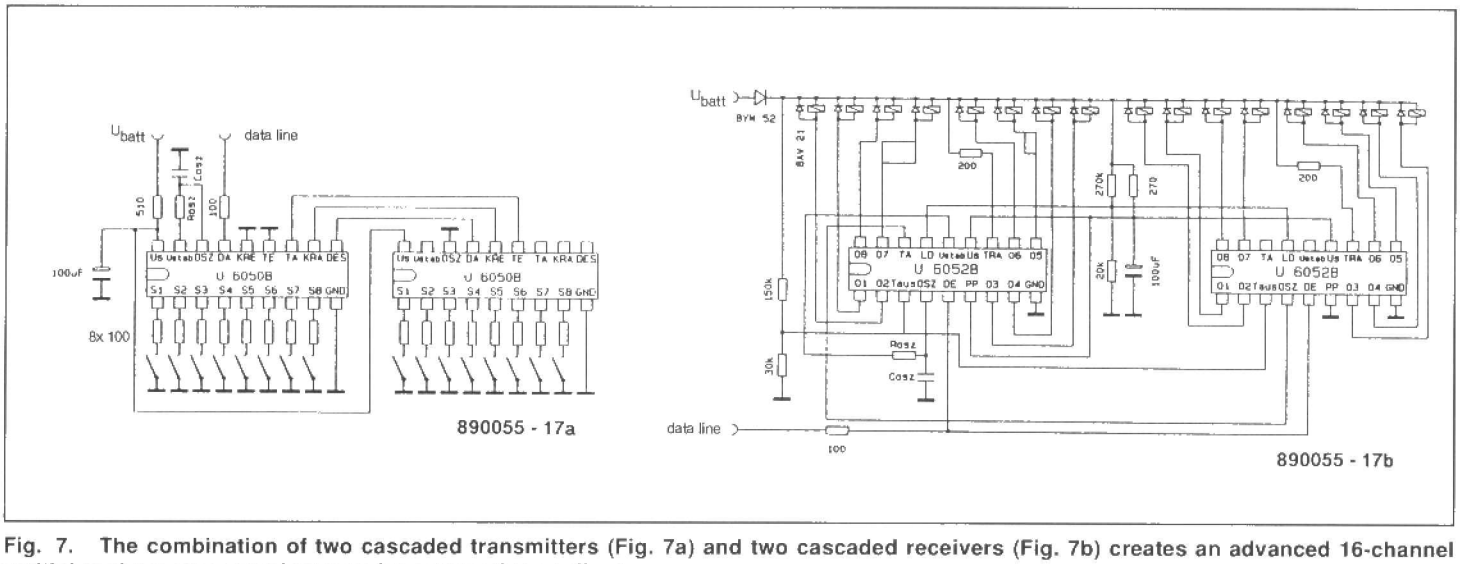


Fig. 7. The combination of two cascaded transmitters (Fig. 7a) and two cascaded receivers (Fig. 7b) creates an advanced 16-channel multiplexed remote control system for automotive applications.

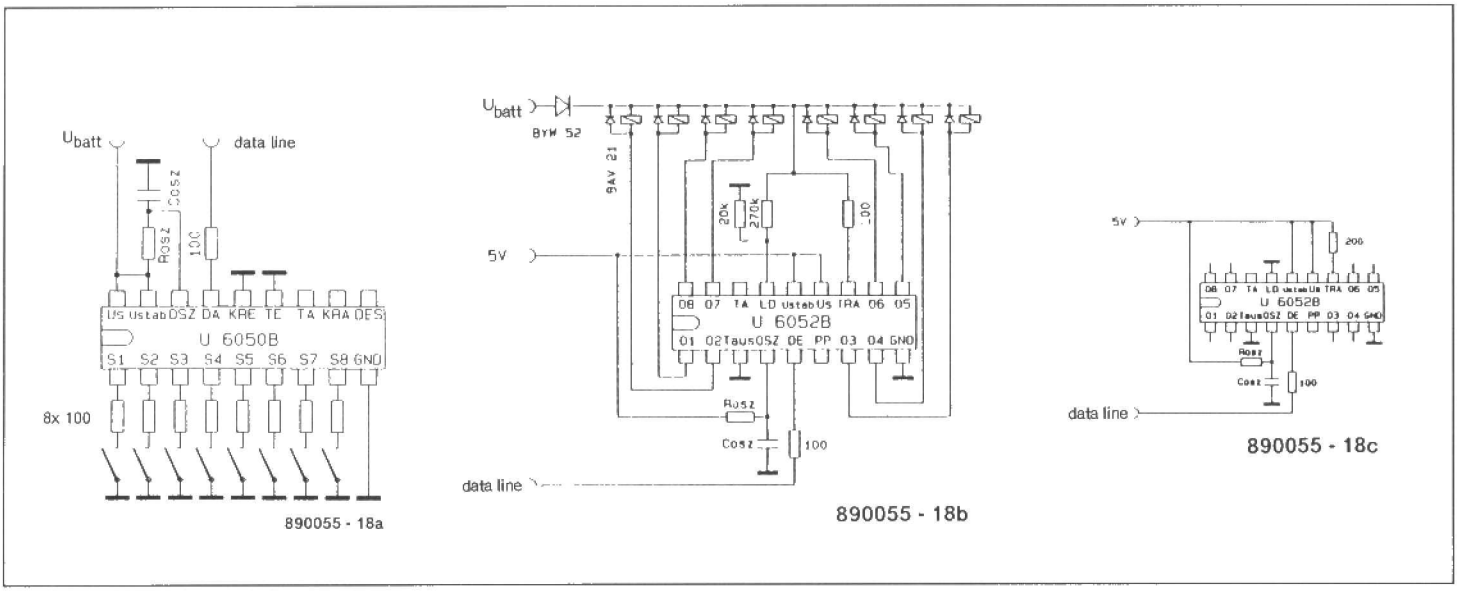


Fig. 8. Illustrating the use of a 5 V power supply: transmitter circuit (Fig. 8a); receiver with relay outputs (Fig. 8b); receiver with open-collector outputs for logic interfacing (Fig. 8c).

the content of the receive register with that of an intermediate latch. When the contents match, the chip increments an internal counter that can count to 4. The same counter is decremented if the register contents are found to be different. The counter is not reset to 1, and the dataword is not transferred to the output buffer, until the counter state is 4, i.e., until equal (= valid) datawords have been received 4 times.

A 'fail-safe' circuit in the U6052B disables the relay driver when, for instance, owing to a short-circuited or broken dataline, transmitter pulses are not received for a period longer than 50 ms. About 35 ms after the data transfer to the output register, a comparator monitors the collector voltage of each actuated relay driver. To afford short-circuit protection, this output is disabled automatically if the measured voltage is found too low. The other functions of the receiver continue to operate normally, however. The maximum output current of the open-collector output transistors in the relay driver circuit is relatively high: about 150 mA. The outputs may be used with voltages up to 22 V.

As already noted, the relay outputs can be clocked. The voltage at pin TAUS defines the mode. Clocking is enabled with TAUS connected to the positive supply rail, and disabled (continuous operation) with TAUS connected to ground. When clocking is used, the clock frequency equals the oscillator frequency of 25.6 kHz at a duty factor of about 0.5. The toggle levels at TAUS are 2.0 V and 2.7 V. The application circuit of Fig. 6 illustrates the implementation of automatic clock disabling when the supply voltage drops below 10 V.

Actuation of the relays under clock control requires fast anti-surge diodes with a relatively high reverse-voltage rating, e.g., the Type BYW52. Along the same lines, it is recommended to use, say, a Type BAV21 diode on the supply line to protect the output transistors in the receiver chip against negative voltage transients and reverse supply voltages.

Another protective measure is implemented at pin LD of the U6052B. When the switching threshold defined with the external resistors is exceeded, the output transistors are turned on fully to enable them to withstand the current through an 80 Ω relay coil.

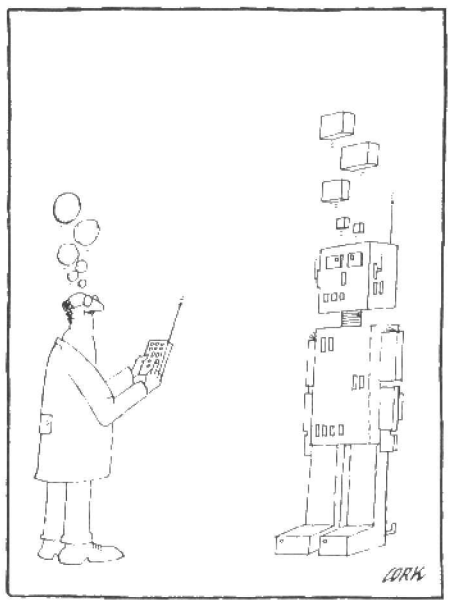
For applications without relay control, the 8 outputs can be used to drive a logic circuit direct if the U6052B is powered from a 5 V supply. The open-collector outputs can be fitted with pull-up resistors to allow direct interfacing with logic circuits operating at a higher or lower voltage than the receiver chip. In this application, the outputs must not be clocked or given a switching threshold (connect both TAUS and LD to ground).

More signals, more chips

The transmitter and the receiver may be cascaded as shown in Fig. 7 to obtain a 16-function multiplexer. The voltage applied to pin PP selects between master (PP = +), single (PP = open) or slave (PP = gnd). The master supplies the clock to the slave chip, both at the receiver and at the transmitter side.

Telefunken Electronic GmbH • Semiconductors Division • P.O. Box 1109 • D-7100 Heilbronn • West-Germany. Telephone: +49 7131 67-0. Fax: +49 7131 67 2340. Telex: 728746 tfk g.

AEG (UK) Ltd • 217 Bath Road • SLOUGH SL1 4AW. Telephone: (0753) 872101. Fax: (0753) 872176. Telex: 847541.



THE DIGITAL MODEL TRAIN – PART 8

by T. Wigmore

Construction & testing

IC sockets may be used, but it should be noted that this is no longer accepted practice, at least as far as standard logics circuits are concerned. Some sockets are more expensive than the IC itself and, more importantly, the reliability of a circuit is inversely proportional to the number of connexion s. None the less, for the more expensive ICs, such as the A-D converter (IC25) and the EPROM (IC13), a good-quality socket is recommended. Bear in mind also that the printed-circuit board is through-plated: any desoldering of ICs is, therefore, a tricky operation. So, check and double-check whether the IC is the correct one before soldering it on to the board.

The parts list shows ICs of the HC- and HCT-type. The HC-types may be replaced by HCT-types, but HCT-types should NOT be replaced by HC-types.

Power supply. Start by fitting D38–D41, D36, C24, C25 and C27. Next, fit IC29 on to the relevant heat sink and mount the resulting assembly on to the board. There are tracks underneath the heat sink that are protected by a thin layer of lacquer only: it is therefore necessary to give these extra insulation (by, for instance, a suitably-sized piece of thin cardboard or old PCB or insulating tape). The IC should be fixed to the heat sink with an M-3 bolt, nut and washer, and a generous amount of heat conducting paste.

Connect the mains transformer to the ~ terminals on the PCB. If you intend to use more than 10 keyboards in addition to the main board, a transformer of higher rating than indicated in the parts list must be used, or the keyboards (dealt with in Part 9) must have a separate power supply. Assuming that the keyboards will be fed by the present supply, wire link A must be fitted.

It is possible to use a suitable mains adapter provided this delivers 9 V at not less than 800 mA. If the adapter delivers a direct voltage, D39 and D40 may be replaced by wire links and D38 and D41 must be omitted.

Switch on the mains and check that the output voltage of IC29 is 5 V ±5%. If it is not, disconnect the mains, discharge C25 via a 100 Ω resistor, and check all the components and the preceding work thoroughly. If the output is all right, switch off the mains and discharge C25 via a 100 Ω resistor.

Oscillator. Fit IC8, IC21, R2, R3, C22, C37, C40 and the crystals on to the board. Switch on the mains and verify that a symmetrical signal of 2.458 MHz exists on pin 12, and a signal of 614 kHz on pin 8 of IC8.

Microprocessor. Fit IC4, R8, R12, R18, R19, R24, C34, D34 (observe polarity!), T1, IC24, R13 and C23. These components constitute the power-up reset for microprocessor IC4. The operation of IC4 is tested by placing an instruction on the data bus by means of hardware. In the first instance, this is the STOP instruction (76_H: 01110110_B). For

Parts list

Resistors:
R1 = 100Ω
R2;R3 = 4k7
R4;R5;R11;R12;R17–R20;R22;R23;R24 = 10k
R6;R10 = SIL resistor array 10k
R7;R8;R15 = 330Ω
R9;R14;R16 = 47k
R13 = 15k
R21 = 6k8

Capacitors:
C1–C16 = 10n (pitch 5 mm)
C17 = 47p
C18;C19 = 100µ; 25V
C20;C21 = 220n
C22 = 33p
C23 = 4µ7; 6V3; tantalum
C24;C27 = 470n
C28–C42 = 100n (pitch 7.5 mm)
C25 = 2200µ; 16V; axial
C26 = 10µ; 6V3; tantalum

Semiconductors:
D1–D32;D37 = 1N4148
D33 = green LED
D34 = red LED
D35 = yellow LED
D36 = 1N4001
D38–D41 = 1N5401
T1;T3 = BC557
T2 = BC547
IC1 = 74HC(T)245
IC2 = 74HC(T)74
IC3 = Z80PIO (Z8420 or Z84C20)
IC4 = Z80CPU (Z8400 or Z84C00)
IC5;IC6 = 74HCT238
IC7 = 74HCT139
IC8 = 74HCT93
IC9 = MC1489 or SN75189
IC10 = MC1488 or SN75188
IC11;IC26 = 74HCT32
IC12 = Z80CTC (Z8430 or Z84C30)
IC13 = 2764 (ESS572)
IC14 = 6264
IC15 = 78L12
IC16 = 79L12
IC17;IC19 = 74HCT174
IC18 = 4066
IC20 = 74HCT244
IC21 = 74HCT04
IC22;IC23 = 74HCT374
IC24 = 74HCT74
IC25 = ADC0816
IC27 = MC145026
IC28 = 74HCT138
IC29 = 7805

Note: ICs from the HC-series may be replaced by HCT-equivalents. Do not use a HC type if a HCT type is stated. LS-types are not suitable because of their higher current consumption.

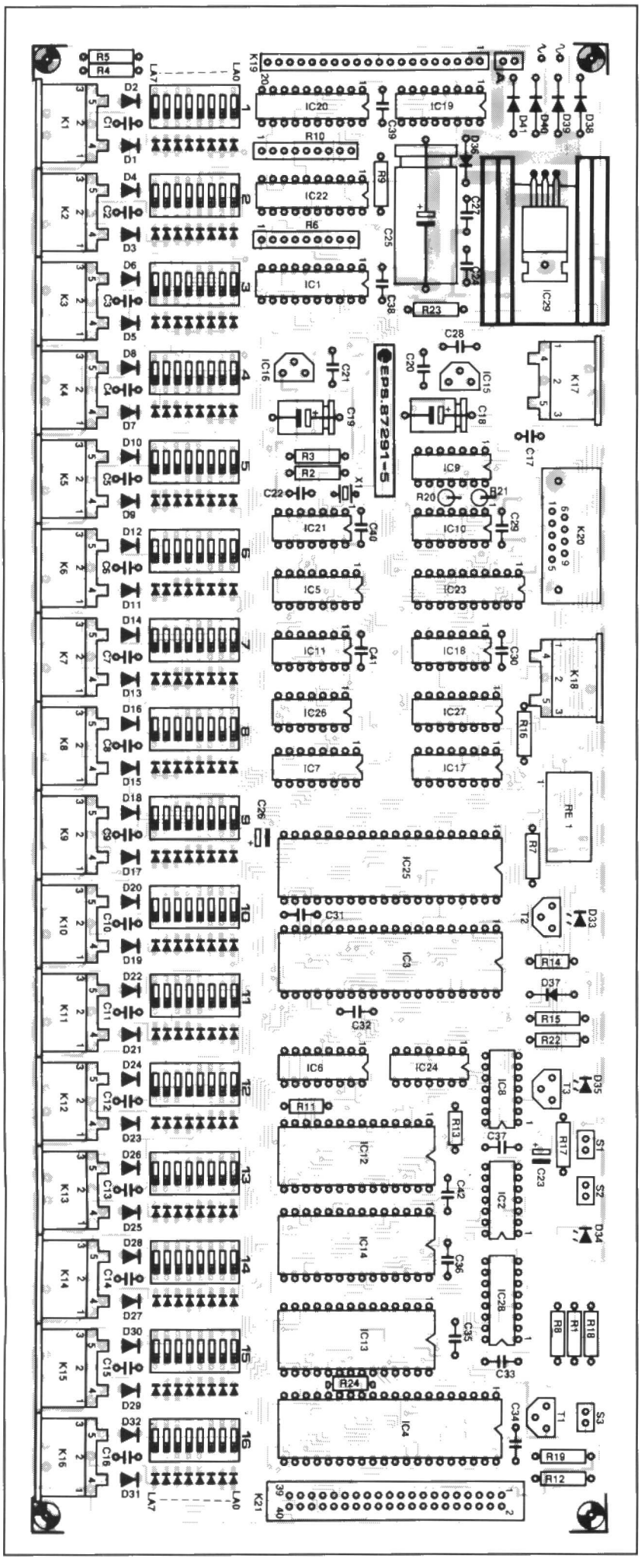
Miscellaneous:
K1–K18 = 5-way 180° DIN socket for PCB mounting*.
36 off M2×5 screws for securing K1–K18.
K19 = 20-way SIL female header; angled; 0.1-in. pitch (e.g., Assmann AWRF A20Z).
K20 = 9-way feamle sub-D connector; angled; for PCB mounting.
2 off M3×8 screws for securing K20.
K21 = optional 40-way for future extensions.
RE1 = DIL reed-relay; 5 V coil voltage; e.g., Siemens V23100-V4005-A000.
X1 = quartz crystal 4.9152 MHz.
S1;S3 = push-to-make button.
S2 = push-to-break button.
Heat-sink for IC29: size 30×37.5 mm (e.g., SK09 from Dau Components/Fischer).
Mains transformer 8 V or 9 V @ 1 A min. sec.
PCB Type 87291-5 (see Readers Services page).

Additionally required for each loco controller (max. 16 allowed):

Loco controller:
Potentiometer 100k linear (rotary or slide type) with knob.
5-way DIN-plug; 180°.
One (EEDTS) or two (Märklin-system) SPST switches.

Loco address settings (4 options):
1) fixed address setting:
diodes 1N4148, max. 6
2) variable address setting:
8 diodes 1N4148 and 1 8-way DIP switch block.
3) variable addresss setting:
8 diodes 1N4148
16-way header with 2×8 contacts in 0.1-in. raster.
max. 6 jumpers
4) extra-flexible address setting:
as option 3 but instead of jumpers:
16-way flatcable connector
2 BCD-encoded thumbwheel switches

* number of sockets depends on number of connected loco controllers. Socket K18 is preferably a 6-way type for PCB mounting.



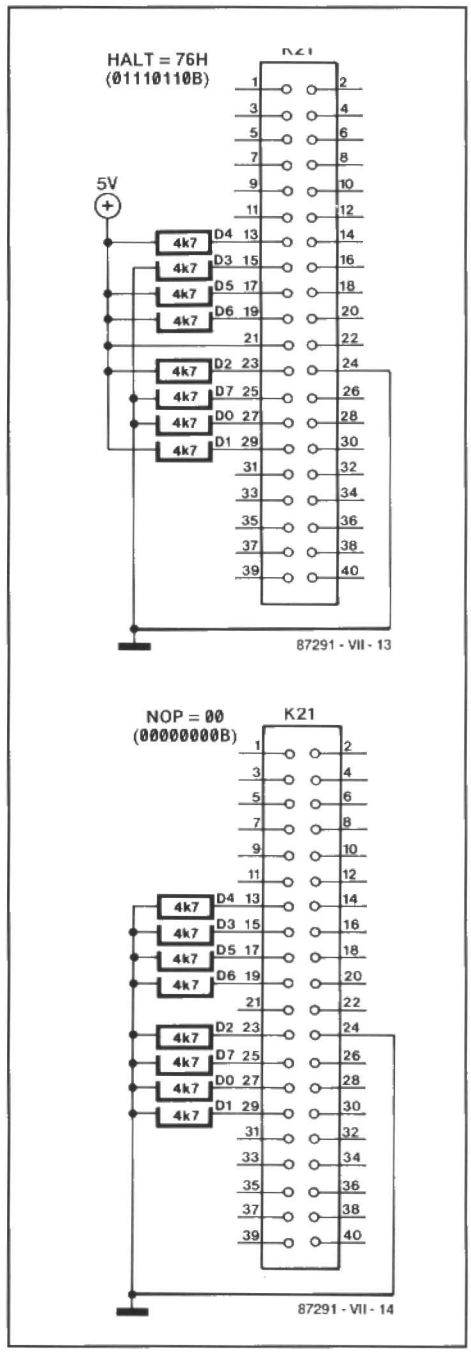


Fig. 49. Operation of the microprocessor is tested by instructions on the data bus formed by resistors. The STOP instruction (01110110_B) is formed as shown at the top, and the NOP instruction (00000000) as shown in the lower illustration.

this, eight 4k7 resistors are connected as shown in Fig. 49a to where later (possibly) K21 will be connected. When the mains is switched on, D34 should light. Switch off the mains and place the NOP instruction (00000000) on to the data bus as shown in Fig. 49b. Switch on the mains and check the data bus for any short-circuits. Pin A0 should have a symmetrical square wave of 307 kHz; A1 one of 307/2 kHz; A2 one of 307/4 kHz; and so on up to A15, which should have one of 9.375 kHz.

Fig. 50. Component layout of the double-sided, through-plated main printed circuit board. The board is illustrated here on a scale of 95:100.

Memory. The next step is the mounting of the EPROM (IC13) that con tains the control program, the RAM (IC14) and the memory address decoder (IC28). At the same time, fit decoupling capacitors C33, C35 and C36. Next, fit IC3, IC12, R11, R16, R17, R9 (immediately adjacent to C25), R22, R15, D35, T3, IC7, IC26, C32, C41, C42, S1 and S2.

Switch on the mains and press S1, when the program should go into the service routine, indicated by the flashing in a 1 Hz rhythm of D35. If this happens, IC3, IC12, IC4 and the memories work satisfactorily. If, however, D33 lights, the control program has gone into the internal RAM test routine: this is almost certainly caused by IC13 and associated components.

Serial output. Fit IC11, IC17, IC18, IC23, IC27, C30, R7, R14, D33 and T2. Switch on the mains and press S1: a low-frequency square wave should then be present at pins Q0 to Q7 of IC23. The frequency of that signal at Q0 should be 1 Hz and that at successive output pins should be one half of that at the preceding pin.

Pin Q0 becomes alternatively high and low every half second; Q1 every second; Q2 every two seconds; and so on. These frequencies were chosen this low to enable them to be checked with an ordinary multimeter. A similar check must be carried out at the outputs of IC17. Again, the first output becomes alternatively high and low every half second and the last one, Q6, every 16 seconds. Note that D35 flashes in unison with output Q0 of IC23, and D33 in unison with Q6 of IC17.

±12 V supply. The ±12 V supply is used not only for the RS232 interface, but also for the booster. It is, therefore, required even if the RS232 interface is not used.

Fit C18–C21, IC15 and IC16. The input voltage for the supply (±20 V) is taken from the booster board (see Part 6 - September 1989) and connected via K17. This connector is shown in the parts list as a 5-way DIN socket, but a (hard-to-obtain) 6-pin type is preferred, because this prevents the connecting cable from being plugged into one of the other DIN connectors by accident. Because of the presence of the ±20 V potentials that would almost certainly have disastrous consequences.

The wires in the cable between the main board and the booster board must be connected to identically-numbered pins on K1 and K17. If a 6-way type (which has different pin numbers) is used for K17, stick to the numbers given on the boards.

Switch on the mains to the booster unit (NOT to the main board). The potential at pin 1 of K18 (with respect to pin 2) should be –20 V and that at pin 3 (again with respect to pin 2) should be +18 V. The output voltage of IC15 should be +12 V and that of IC16, –12 V.

A-D converter and locomotive address decoder. Fit R1, R4, R5, C26, C31, C38, IC1, IC2, IC25 and resistor-array R6. Instead of an array, eight 10 kΩ resistors may be fitted vertically as shown in Fig. 51. Note that the common earth connexion must be at the underside.

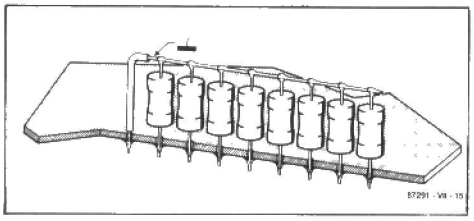


Fig. 51. Instead of resistor-arrays R6 and R10, eight 10 kΩ resistors may be fitted vertically.

To enable writing the loco addresses associated with the loco controllers, IC6 and (if more than eight loco controls will be used) IC5 are needed. Loco controls may then be connected to K9–K16. The controller with the highest connector number has the highest priority if the addresses are coded identically. In other words, if in positions 10 and 14 the controllers have the address 00, that in position 14 will have priority over that in 10.

Construction of a loco controller. The A-D converter can not be tested until a loco controller is available. From a circuit point of view, these controllers are fairly simple: three possible designs are shown in Fig. 52. For each of these designs a 5-way DIN plug (180°), a 100 kΩ potentiometer and one or two switches are required. Note that the housing of the DIN plug is used as the sixth (earth) pin.

It is possible to connect the loco controllers direct to the main board, i.e., without plugs and sockets. This is a particularly logical (and less expensive) method for controllers that are to be built in permanently.

Each loco controller is associated with one or two switches for the switching on and off of the controller, the setting of the type of data format and, possibly, the additional decoder switching function.

If a mixture of Elektor Electronics and Märklin loco decoders is used, the controller design shown in Fig. 52a should be used. The design in Fig. 52b is intended for Elektor Electronics controllers and that in Fig. 52c for Märklin or the modified Elektor Electronics controller (see Part 3 - April 1989).

A controller is considered to be out of action if both pin 4 and pin 5 of the DIN connector are open and therefore also if the relevant DIN connector on the main board is not connected up.

Switch S1 in Fig. 7b and 7c may be replaced by a wire link at the relevant DIN connector. A controller can then be taken out of action only by removing the plug from the DIN socket.

If the connexions between the main board and the controllers are fairly long, it is recommended to use screened cable.

Each loco controller needs a filter capacitor and two diodes, all of which may be fitted on the main board.

Diodes D1–D32 must be fitted vertical-

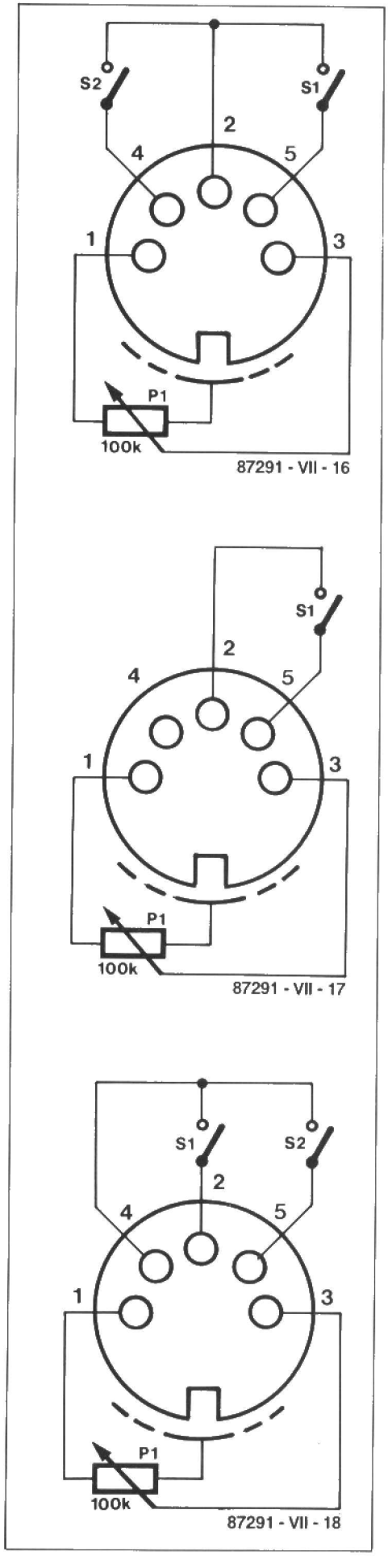


Fig. 52. Three possible designs of a locomotive controller. Choice of the design depends on the type of locomotive decoder used.

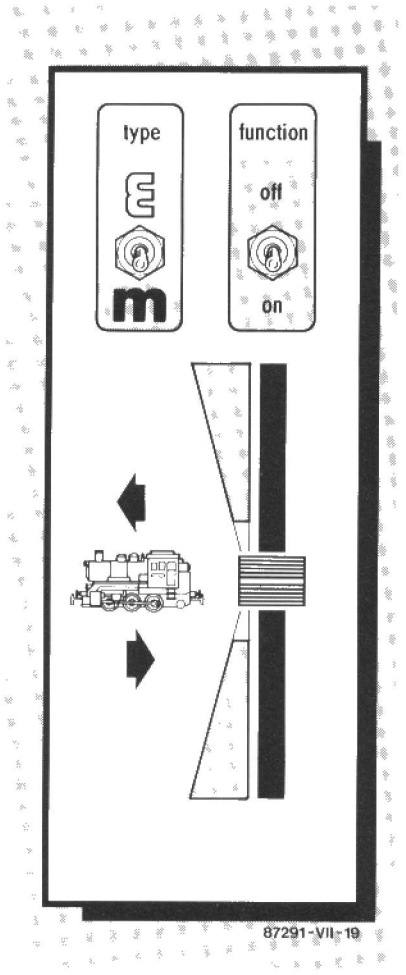


Fig. 53. Possible design of a front panel for the loco controllers.

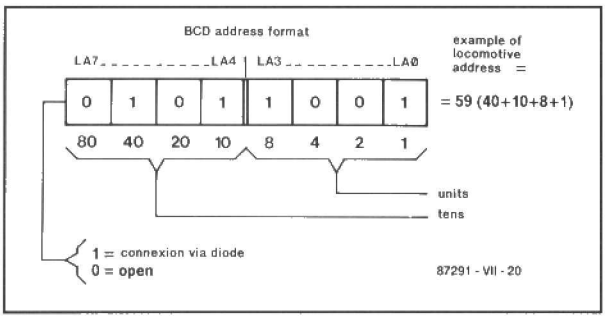


Fig. 54. Loco addresses (00–80) must be presented in BCD format.

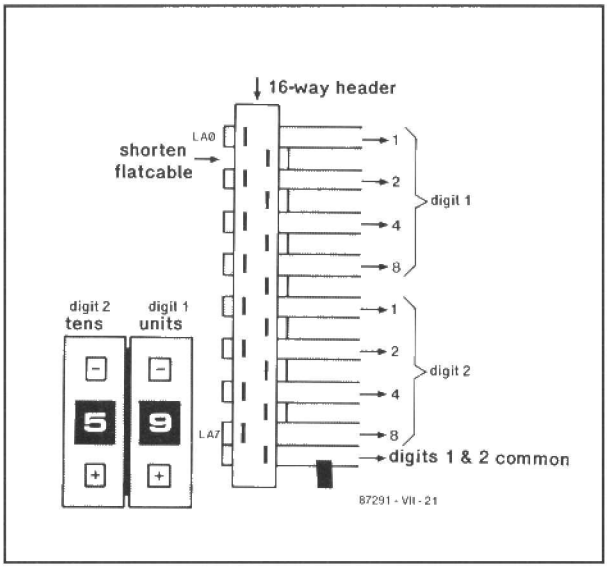


Fig. 55. Thumb-wheel switches may be connected via flatcable. Unused wires should not be connected to prevent unnecessary capacitive loads.

ly.

Since the DIN sockets are subject to fairly large mechanical strains during the insertion and withdrawal of plugs, they should be fixed to the board with M2×5 nuts and bolts or with small self-tapping screws before the solder connexions are made.

Loco controllers and the A-D converter may be tested by connecting them to K16, which is the most important loco controller socket. The setting of the loco addresses will come later: for the time being, they will be written as 00.

Switch on the mains to the main board, but do NOT press S1. The normal control program will then be active. After a moment or two press S1 when D33 should light. Also, the signals resulting from the A-D conversion are present at outputs D3–D7 of IC25, while at pins 6 and 9 of IC2 the switch position may be verified: if the output is 0, the switch is closed and if it is 1, the switch is closed.

Output relay. Fit Re1, D37, IC10, R20, R21 and C29. When the mains is switched on, pin 3 of IC10 should have a d.c. potential of –10 V to –12 V. When S1 ('go') is pressed, the output relay will be energized in unison with the lighting of D33.

Also, the same potential as at pin 3 of IC10 should be present at pin 4 of K17. When in this condition a loco controller is connected, the potential should vary slightly when the potentiometer is adjusted. The degree of the variation depends on the loco address. This voltage is no longer a true d.c. potential as may be verified with an oscilloscope, which will show the repeatedly sent loco control instructions whose rear portion varies according to the position of the potentiometers and function switches, while their front portion varies according to the relevant loco address.

Setting the loco addresses. In general, loco addresses must be presented in BCD format as shown in Fig. 54. Valid addresses are in the range 00–80 (note that Märklin does not count 00 as a valid address). Invalid addresses are simply ignored. A number of possibilities of setting the addresses is shown in Fig. 56.

The method of Fig. 56a is by far the least expensive, but has the disadvantage that addresses can be changed only with the aid of a soldering iron.

The method in Fig. 56b is the one used in the present design. The DIL switches permit setting and altering the addresses at any given moment, even during operation of the system.

It is also possible to program the loco addresses via the RS232 port: this method will be discussed in a later instalment.

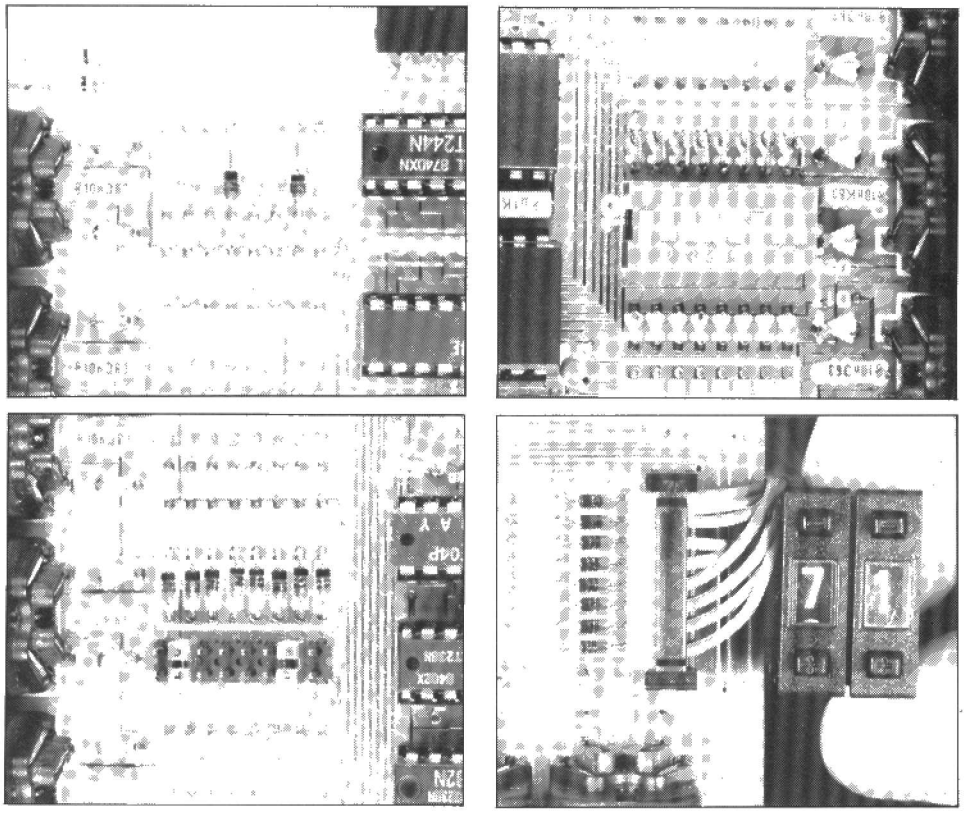


Fig. 56. Four possibilities of setting loco addresses: (a) with diodes (address = 48); (b) with diodes and DIL switches (address = 21); (c) with diodes and shorting plugs (address = 42); (d) with diodes and thumb-wheel switches (address = 71).

Keyboard interface. This section of the board need, of course, only be populated if

it is intended to connect keyboards (which will be dealt with in next month's instalment) to the main board.

Fit resistor-array R10 (but see Fig. 51), R23, C28, IC19, IC20, IC21 and K19. The choice of a single-in-line type for K19 was deliberate, because if the keyboards are installed permanently, they may be connected by means of wire links instead of by relatively expensive plugs.

RS232 interface. To populate the last section of the main board,fit IC9, C17, K20 and K18.

The installation of the main board is left to your own requirements, but bear in mind that keyboards must be connected to the left-hand side of the (flat) case

Some operational tips

Loco controllers are scanned from left to right. If several controllers are set to the same address, the one at the extreme right will have priority over the others.

As in the Märklin system, it is possible to set the speed of one locomotive with a given controller and then use that controller for a different loco address, without affecting the operation of the first loco.

If the mains is not connected to the system and S1 is pressed, the green LED (D33) will light, but go out as soon as S1 is released.

The system can not and will not send data until the booster is switched on and the go key (S1) has been pressed. If the connexion with the booster is broken, the system will automatically come to a halt.

The system ignores brief (< 0.5 s) short-circuits. Again, if the system switches itself off, it may be reactuated by pressing S1.

In emergencies, the system may be stopped by pressing S2: this not only incapacitates the control program, but it also removes the power from the rails. If desired, a number of these stop switches may be installed in series along the track.

Switch S3 is the system reset control, which normally will not be used. Only if the system does not appear to react to any other control or if D34 unexpectedly lights, should this switch be used.

ELECTRONICS SCENE

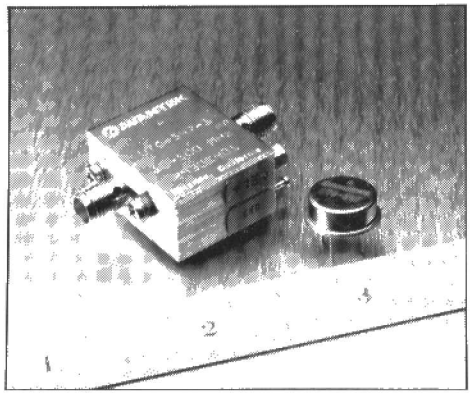
COMPUTERS IN THE CITY

The sixth "Computers in the City" exhibition and conference, organized by Blenheim Online, will be held at the Barbican Centre, London, from 14 to 16 November. The conference programme will focus on the problems facing the systems professional supporting the investment industry and the capital markets.

Further information from Blenheim Online • Blenheim House • Ash Hill Drive • PINNER HA5 2AE • Phone 01-868 4466.

10–500 MHZ MODULAR AMPLIFIER

Avantek is introducing a 10–500 MHz thin-film amplifier that features high dynamic range (+31 dBm two-tone, 3rd-order intercept point), high output power (+19 dBm), and low noise figure (2.8 dB), combined with 12.5 dB and 0.2 dB full-band flatness (all typical at +25 °C).



Also announced are a 2–16 GHz transistor with noise figure comparable to that of today's commercially available HEMT devices, but fabricated in proven, reliable GaAs technology, and a 2–6 GHz general-purpose GaAs MMIC that features 12.0 dB gain, ±8 dB full-band gain flatness, +12 dBm output power at 1 dB gain compression (all typical) and operates from a single +12 V d.c. supply voltage at 65 mA Details (in UK) from Wave Devices • Laser House • 132–140 Goswell Road • LONDON EC1V 7LE. For other countries see *Elektor Electronics*, January 1988.

BRITISH AMATEUR RADIO TELEDATA GROUP

Two of BARTG's mainstays, Pat and John Beedie (GW6MOJ and GW6MOK) are retiring from the BARTG committee. From 4 November (the date of BARTG's AGM), Ann Reynolds (G6ZTF • 169 Bell Green Road • COVENTRY CV6 7GW) will become membership| secretary. On the same date, Ted Hatch (G3ISD • 147 Borden Lane • SITTINGBOURNE ME10 1BY) will take over the sales of components and software, while publications will then be available from BARTG's editor, Peter Adams (G6LZB • 464 Whippendell Road • WAT-FORD WD1 7PT.

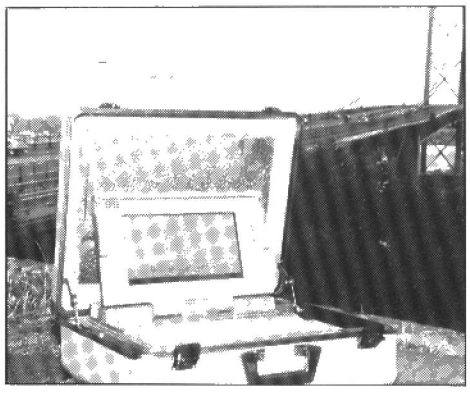
NEW FACTORY FOR EUROQUARTZ

One of Britain's leading crystal companies, Euroquartz, has opened its new purpose-built factory at Crewkerne to enable its production capacity to keep pace with demand.

At the same time, the company has announced a new range of tight tolerance 14-pin DIL oscillators. These new devices have a frequency tolerance of ±25 ppm and are available in the frequency range of 3.5 kHz to 64 MHz.

As well as servicing the volume requirements of quartz crystal components as popularly used in the electronics industry via distribution, Euroquartz has grown its manufacturing facility. The components now available from the company cover all popular microprocessor crystal and oscillator frequencies, TCXO, VCXO,OCXO devices, made-to-order crystals and oscillators, as well as more esoteric devices such as real-time clock oscillators, programmable oscillators, special filters and custom-designed frequency products.
Euroquartz Ltd • Blacknell Lane Industrial Estate • CREWKERNE TA18 7HE.

RUGGEDIZED VERSION OF ITS LAPTOP PC



ITS have released a ruggedized version of their laptop PC, designed specifically for field and factory applications, such as sound and vibration monitoring, where extended battery life and resistance to harsh environments is essential. The portable PC is shock-mounted in a rugged but lightweight aluminium case and battery capacity has been extended to give 15 Ah operation with an integral charger for overnight recharge.

The ITS portable has up to two full-length internal slots for add-in PC compatible cards and with its enhanced battery storage, even add-in cards with relatively high power consumption can be used remotely.
Integrated Technology Systems Ltd • 5 Holyrood Avenue • GLENROTHES KY6 3PF.

3½-DIGIT SMD VOLTMETER

T. Wigmore

This little circuit is simple to build, offers good accuracy and can be used in all applications requiring a small voltmeter with a clear LED read-out.

Much of today's electronic equipment requires a digital read-out to show system status or process variables. Such read-outs are usually compact voltmeter modules with an LC (liquid crystal) display. The present read-out is also a voltmeter, but uses displays with light- emitting diode (LED) segments. A LED indication was chosen for this application because it remains visible in the dark (this requirement would also have been met by an LCD with back-lighting). Also, the use of 7-segment LED displays in combination with a drive circuit built with SMA (surface-mount assembly) components allows a really compact voltmeter to be realized — see Fig. 1. This is particularly important if the meter is to be built into existing equipment.

One integrated circuit

The circuit (Fig. 2) is formed by a single integrated circuit Type ICL7107 from Intersil. This voltmeter IC is the LED version of the perhaps even more familiar ICL7106 for LCDs. The ICL7107 contains everything required for the analogue-to-digital conversion of the input signal, and the driving of a 3½-digit read-out. The chip is used in a more or less standard application circuit with some extra components to afford flexibility as regards the power supply.

Analogue-to-digital conversion

Analogue-to-digital (A-D) conversion can be accomplished in a number of ways. Fast converters almost invariably use

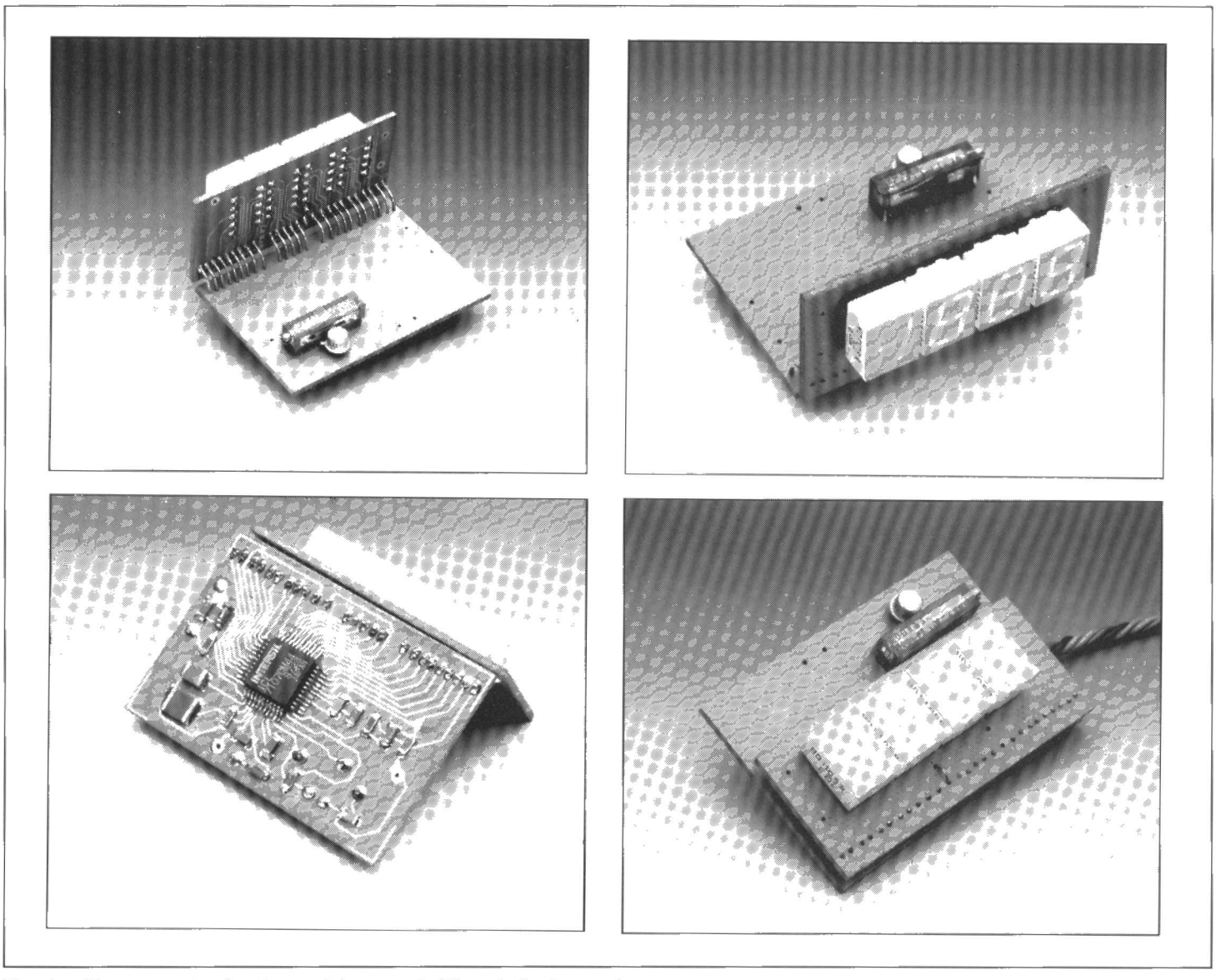


Fig. 1. The compact voltmeter module seen at different viewing angles.

flash ADC chips that are characterized by a large number of internal comparators. The other principle, successive approximation, is based on a resistor ladder network whose R-2R junctions are connected to counter outputs. The result of the D-A conversion is compared to the input signal. If a difference is detected, the clock oscillator with the counter is controlled accordingly until the output voltage of the internal D-A converter equals the externally applied voltage. In practice, the accuracy of this type of converter is that of the R-2R network, and the off-set voltage of the voltage comparator.

The ICL7107 and other ICs in its family work on yet another principle, which is entirely analogue and based on an integrator. Internal off-set voltages are compensated prior to any measurement cycle, so that a high accuracy is achieved even with small input voltages. Since the measurement principle is based on the comparison of an input voltage, U_i, with a reference voltage, U_{ref}, the display value is in fact U_i/U_{ref}. Interestingly, the reference voltage may be applied externally.

Three phases

The measurement cycle of the ICL7107 consists of 3 phases. Figure 3 shows the signal path in the analogue input circuit for each of these.

During the auto-zero phase (Fig. 3a), inputs IN LO and IN HI are disconnected. Internally, a closed loop is formed consisting of input buffer amplifier A_1, integrator A_2 and comparator A_3 (C_{int} is discharged as yet). The internal ground is formed by the analogue common potential. The auto-zero capacitor will charge to a voltage that compensates the off-set voltages of A_1, A_2 and A_3. Also, C_{ref} is charged to the reference potential.

The auto-zero phase is followed by the integration phase. The input voltage between IN LO and IN HI is applied to an integrator formed by A_2-R_{int}-C_{int}. The integration interval is defined as 1,000 clock cycles. During this interval, the output voltage of the integrator rises to a value directly proportional to the input voltage.

The last phase is the de-integration phase. The input voltage to the integrator is disconnected again and replaced by the voltage on C_{ref}. An internal circuit allows the reference voltage to be connected with the opposite polarity of the previously applied input voltage. This causes the integration process to be reversed, and the interval to be timed by the internal clock. The number of clock pulses is directly proportional to the ratio of the reference voltage to the input voltage. This principle is best understood by assuming the reference voltage to be equal to the input voltage, which results in a de-integration phase that is just as long as the integration phase. The length is 1,000 clock cycles, which is shown on the display. If the input voltage is only half the reference voltage, the de-integration process takes half the time of the integration process, and the display will read 500 to indicate that $U_{in} = 0.500U_{ref}$.

The length of the de-integration phase depends on the input voltage. With relatively long de-integration phases, the auto-zero phase is automatically shortened so that the total measurement time — and with it the number of read-outs per second — remains constant. The integration phase always lasts 1,000 clock cycles, the de-integration phase 0 to 2,000 clock cycles, and the auto-zero phase 1,000 to 3,000 clock cycles. One complete measurement cycle takes 4,000 clock cycles, bearing in mind that the clock frequency is divided internally by 4. A clock frequency of 48 kHz gives an internal clock frequency of 12 kHz to allow 3 measurements per second.

Common mode

The dual slope measuring principle used by the ICL7107 has been discussed in some detail to show up the limitations of the common-mode arrangement.

Clearly, satisfactory measurements can be made only if the reference and input voltages lie within common mode range, V−(+1 V) to V+(−0.5 V), of the internal amplifiers. Another requirement is for the integrator output voltage to remain well below the positive supply voltage. During the integration phase, the

3½-DIGIT SMD VOLTMETER

• Read-out:	3½-digit LED display
• Sensitivy:	±200 mV; differential input with symmetrical supply
• Decimal point:	2 positions; indication 188.8 or 18.88
• Reference:	internal or external
• Supply voltage:	single 5 V (limited common-mode); 5 V with negative bias; symmetrical (±5 V)
• Current consumption:	max. 200 mA from positive (+5 V) supply; 300 µA from negative supply
• Size:	55×37×11 mm

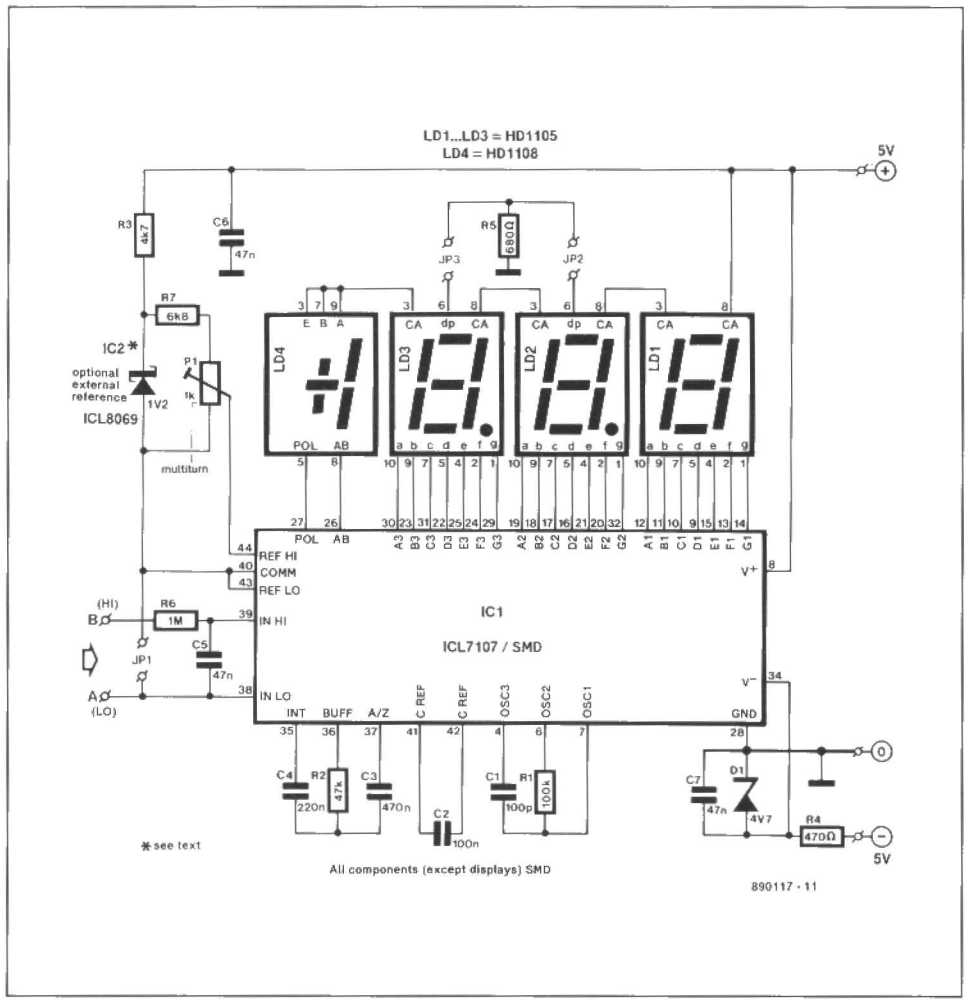


Fig. 2. Circuit diagram of the voltmeter.

voltages at IN LO and IN HI are connected to the inputs of the internal buffer amplifier and the integrator, and must, therefore, fall within the common-mode range. The reference voltage is never applied direct, but via the previously charged capacitor C_{ref}. This means that the common-mode voltage range (CMVR) of the reference voltage is the supply voltage, i.e., V+ to V–.

During the integration phase, the integrator uses the potential at IN LO as the reference. De-integration, however, is effected with respect to the 'common' potential. Consequently, any difference between the IN LO potential and the common potential causes a voltage jump at the integrator output during the switch-over from integration to de-integration (see Fig. 3b).

Displays

In the circuit diagram in Fig. 2, the oscillator frequency is set to 48 kHz by components C_1-R_1. This frequency results in 3 read-outs per second, and may be adapted to individual requirements by changing R_1-C_1 as appropriate, bearing in mind that the integrator time-constant, R_2-C_4, must be changed at the same time.

Input filter R_6-C_5 ensures a stable read-out.

The segment current capability of 5 to 8 mA of the ICL7107 obviates additional driver transistors and current limiting resistors. The read-out is composed of 3 common-anode 7-segment LED displays Type HD1105, and 1 common-cathode display Type HD1108. The latter is used because ½-digit, 12.7 mm-high, LED displays are difficult to obtain in common-anode versions. Fortunately, the cathode of the minus sign on the HD1108 is not connected to the A and B segment. Both the HD1105 and HD1108 are manufactured by Siemens.

Internal and external reference

The internal reference source of the ICL7106 and the ICL7107 may be used with a sufficiently high supply voltage (more than 6.5 V between V– and V+). The temperature characteristics of this reference may, however, cause problems with the SMA ICL7107 because this is a relatively small chip, and drives LEDs direct. For this reason an external reference, e.g., the ICL8069, may be used. Other reference devices may be used provided R_3 is modified accordingly to ensure optimum bias current (note that the voltage difference between REF LO and V+ is typically 2.8 V). Resistor R_7 has a value that allows multiturn preset P_1 to be adjusted to give a reference voltage of 100 mV between REF LO and REF HI.

Construction

The printed-circuit board (Fig. 5) accommodates the voltmeter circuit and the displays. The board is cut in two to enable the display section to be mounted either vertically or horizontally on to the voltmeter board.

All components, except the optional reference, IC_2, multiturn preset P_1 and the 4 displays, are surface mount assembly (SMA) types.

The values of R_3 and R_7 depend on whether or not IC_2 is used, while components R_4, C_7 and D_1 may be required only with certain power supplies as discussed below.

The two jumpers on the board allow the decimal point to be positioned either between the first and second digit (e.g., 100.0) or between the second and third digit (e.g., 10.00). The third option, 1.000, is not possible because the fourth digit is a common-cathode type.

Power supply

In most cases, the voltmeter will be incorporated into an existing piece of equip-

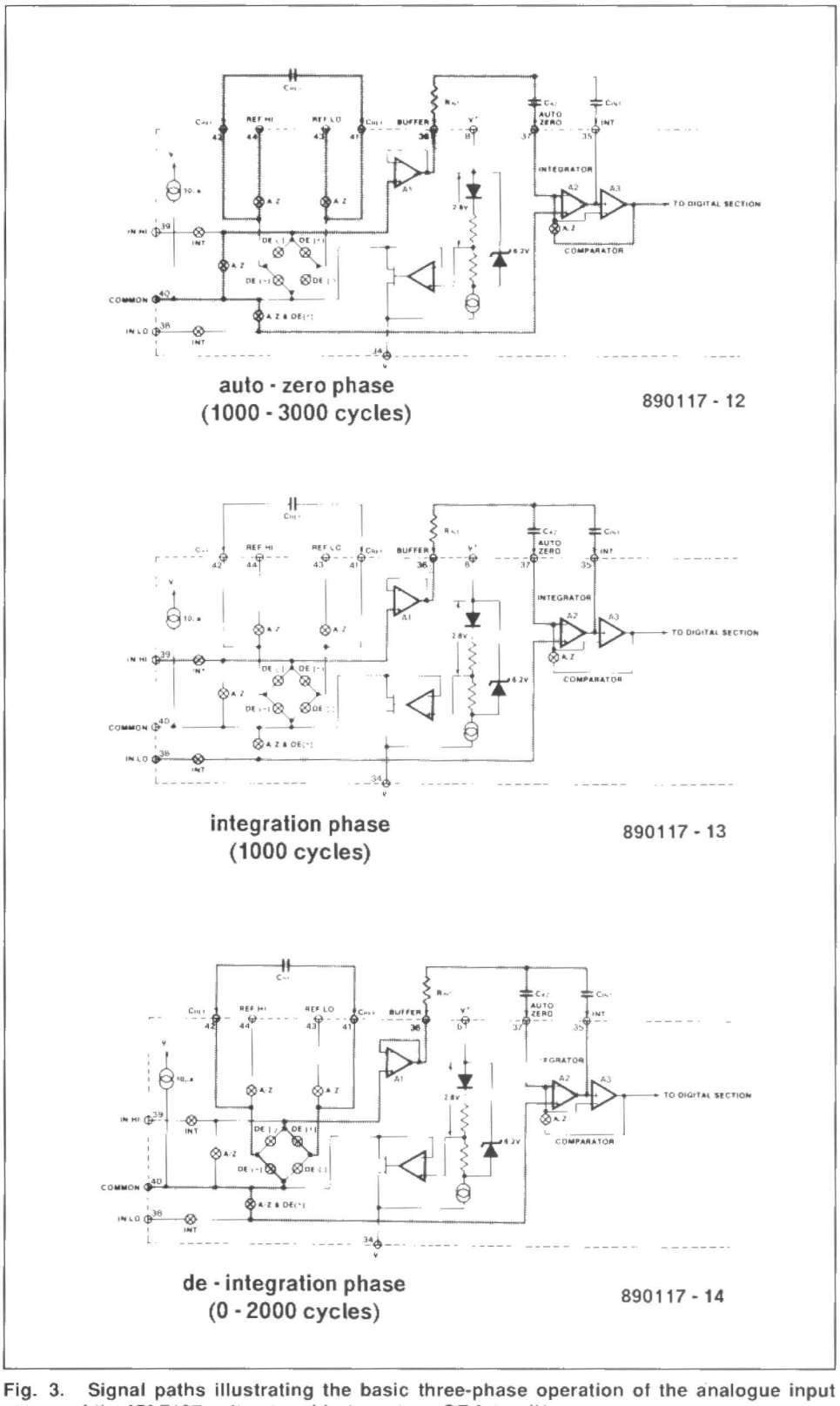
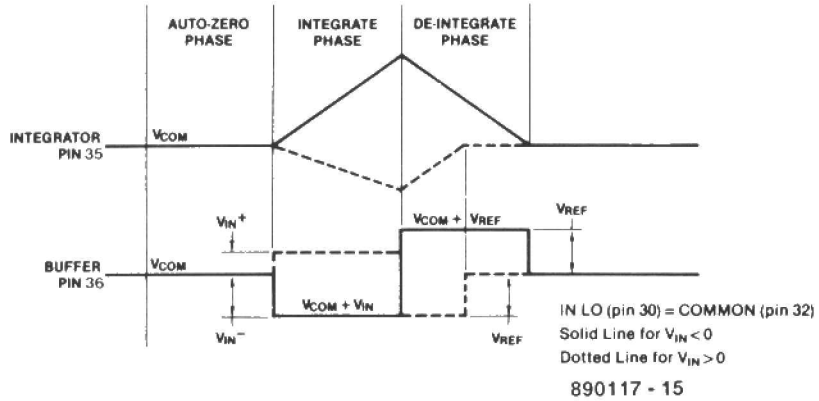


Fig. 3. Signal paths illustrating the basic three-phase operation of the analogue input stages of the ICL7107 voltmeter chip (*courtesy GE-Intersil*).



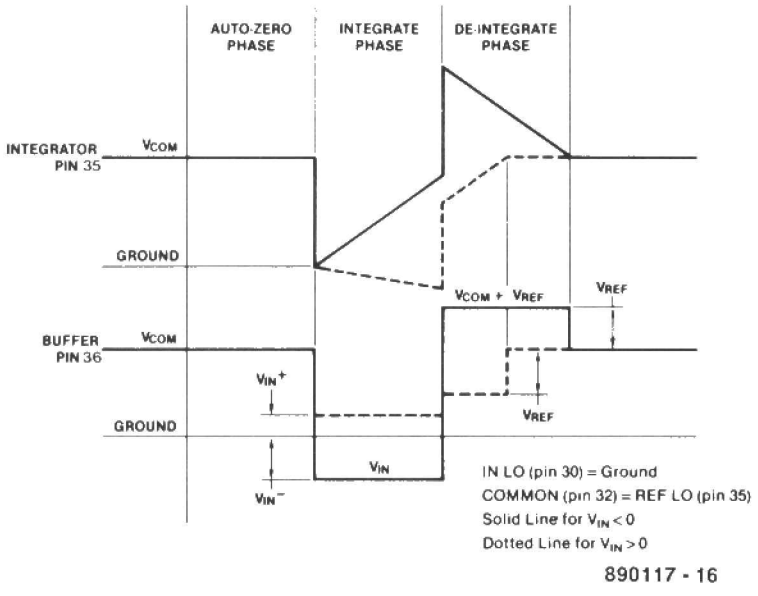


Fig. 4. Signal waveforms with terminals LO an COMMON connected (top drawing) and with a potential difference between LO and COMMON (lower drawing) (*courtesy GE-Intersil*).

Parts list

All parts surface-mount assembly except when marked +.

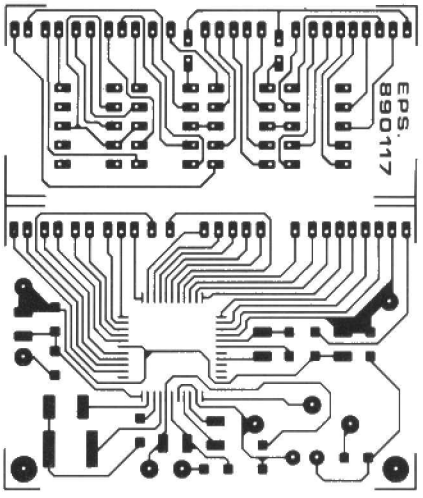
Resistors:
R1 = 100k
R2 = 47k
R3 = 4k7
R4 = 470Ω
R5 = 680Ω
R6 = 1M0
R7 = 6k8
P1 = 1k0 multiturn preset +

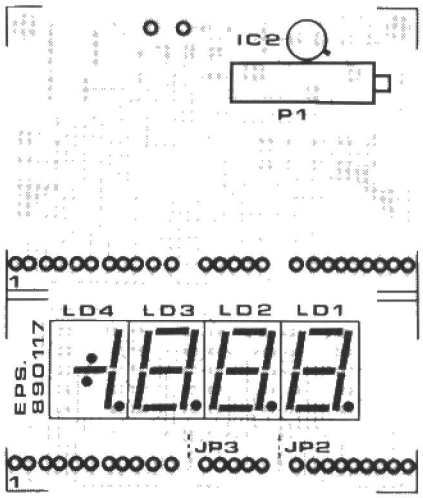
Capacitors:
C1 = 100p
C2 = 100n
C3 = 470n
C4 = 220n
C5;C6;C7 = 47n

Semiconductors:
D1 = zener diode 4V7; 400 mW
LD1;LD2;LD3 = HD1105R (Siemens) +
LD4 = HD1108R (Siemens) +
IC1 = ICL7107 (GE-Intersil)
IC2 = ICL8069 (GE-Intersil) +

Miscellaneous:
PCB Type 890117 (see Readers Services page).

SEE ELEKTOR FEBRUARY 1990 P-59 CORRECTIONS FOR 3 DISPLAYS





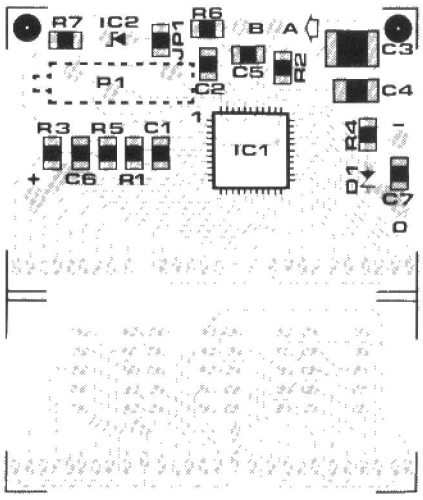


Fig. 5. Track layout and component mounting plan of the printed-circuit board.

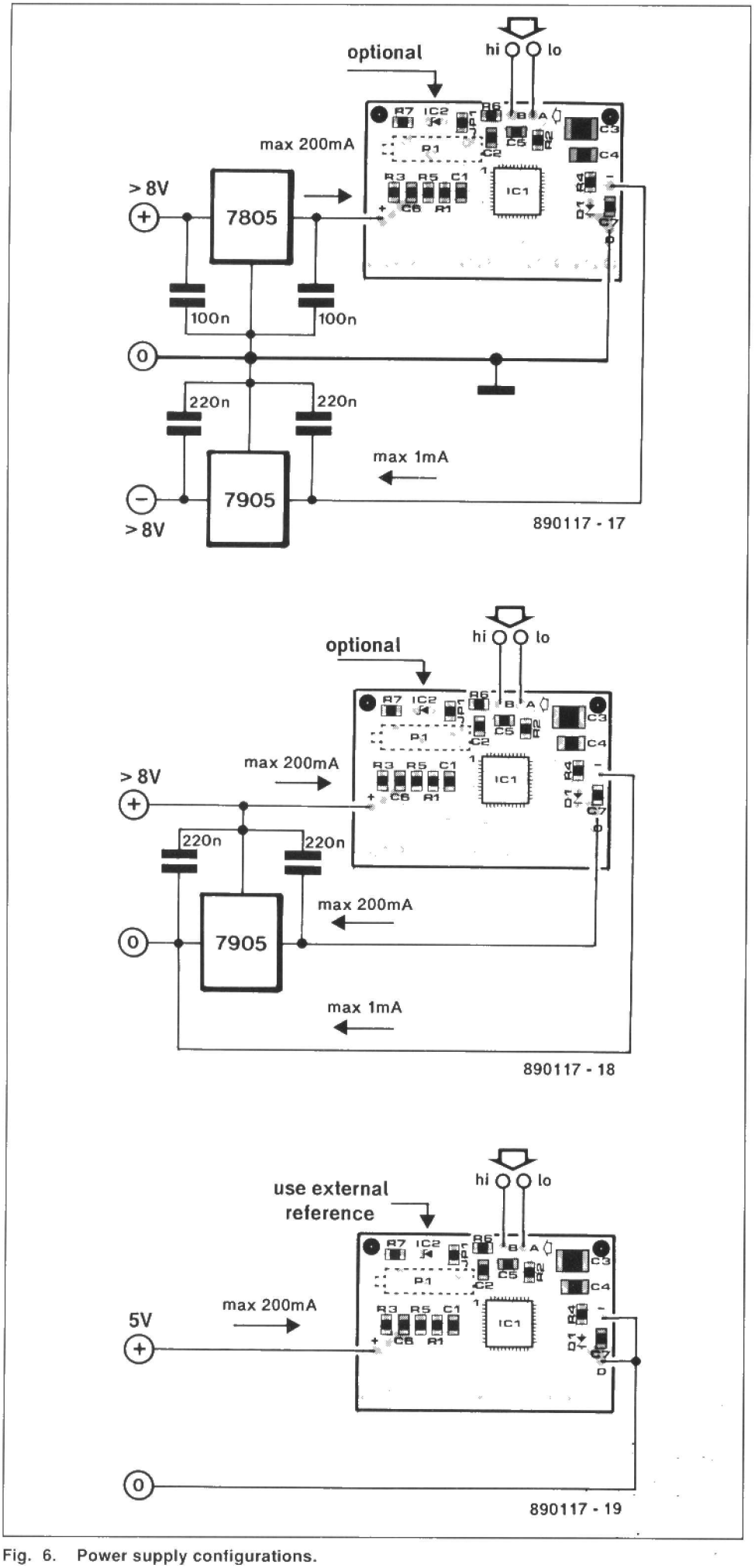


Fig. 6. Power supply configurations.

ment with an internal power supply.

Without displays, the voltmeter draws 1.5 mA at 6 V max. between V+ and ground, and –300 µA at 9 V max. between V– and ground. With displays, the current drawn from the positive supply lies between 70 mA and 200 mA, depending on the number of actuated display segments. The negative supply need not source more than 300 µA, and is not even required in some applications.

The positive supply voltage is limited to prevent the maximum dissipation of the ICL7107 being exceeded.

Figure 6 shows the various supply options. The first drawing, Fig. 6a, shows the most universal solution based on a symmetrical power supply. A 0 Ω or other low-value resistor is fitted in position R_4 (0 Ω resistors are quite common in surface-mount technology), and D_1 is *not* fitted.

The circuit of Fig. 6b may be used if a sufficiently high, regulated, supply voltage is available in the equipment. It should be noted that the input voltage is *not* measured with respect to ground.

Another possibility is shown in Fig. 6c. A single-rail power supply with an output voltage of 12 V or more may be used if the negative supply to IC_1 is limited by fitting D_1 and R_4.

In many cases, a single 5 V supply may be used as shown in Fig. 5d. This application requires the use of the external reference and the fitting of JP_1.

Input voltage and sensitivity

In deciding the range of the input voltage, due account should be taken of the common-mode voltage. Fit jumper JP_1 if the input voltage floats with respect to the display unit.

Non-floating input voltages must lie in the range V–(+1 V) to V+(–0.5 V). When the input voltage is close to V–, the readout, on going negative, may change suddenly to a large value, e.g., –005 instead of 000, –001 etc. This effect may be prevented by shifting the common-mode input voltage towards the middle of the supply voltage.

Set the sensitivity to 200 mV full-scale indication by adjusting P_1 for 100 mV between REF LO and REF HI (the reference voltage is half the full-scale indication). The preset allows small adjustments to be made as required for other sensitivities. If the meter is to be made less sensitive, either an external voltage divider must be fitted, or P_1 must be made larger. The latter solution, however, requires the integrator resistor to be increased accordingly to prevent clipping of the integrator.

PRACTICAL FILTER DESIGN – PART 10

by H. Baggott

This final part of the series discusses all-pass filters. Strictly speaking, these networks are not filters since (ideally) they have zero attenuation at all frequencies. However, they introduce a specific phase shift or time delay that is very useful in many applications.

Although all-pass networks have zero attenuation at all frequencies, they introduce a certain phase shift and act, therefore, as a sort of delay line. They may be used, for instance, to delay a signal in time or to modify the phase behaviour of an other filter.

A look at the complex field of these filters shows that their zeros of network function are mirror images of their poles. Since the poles are always located to the left of the y-axis (because of the required stability of the filter), the zeros must always be to the right of the ordinate. Thus, a first-order network is always a real pole-zero combination.

It is interesting to note that owing to the unique character of an all-pass network the introduced phase shift is always twice the value of that of a conventional filter. The maximum phase shift in a traditional first-order filter is 90°, while that in a first-order all-pass network is 180°.

First-order network

The transfer function of a first-order all-pass network is

$$T(j\omega) = \frac{j\omega - \alpha}{j\omega + \alpha}$$

where α indicates the location of the pole. The absolute value is

$$|T(j\omega)| = \frac{\sqrt{\omega^2 + \alpha^2}}{\sqrt{\omega^2 + \alpha^2}} = 1$$

It is seen that for every frequency the nominator and denominator have the same value. The associated phase shift is

$$\varphi = -2\arctan(\omega/\alpha)$$

The time delay, t, is also important in all-pass filters; it is calculated from

$$t = \frac{d\varphi}{d\omega} = \frac{2\alpha}{\omega^2 + \alpha^2}$$

The time delay in a first-order network is always maximal at very low frequencies and decreases gradually with increasing frequencies. The gradient of the increase depends on the value of α. When α is small, the time delay is large at 0 Hz, but decreases very rapidly with rising frequencies. When α is large, the time delay is relatively small at 0 Hz, but remains fairly constant over a wide range of frequencies.

Second-order network

A second-order filter affords rather more freedom in design, so that the time delay curve can be matched more accurately to the requirement.

The transfer function of this type of network is

$$T(j\omega) = \frac{(j\omega)^2 - j\omega\frac{\omega_r}{Q} + \omega_r^2}{(j\omega)^2 + j\omega\frac{\omega_r}{Q} + \omega_r^2}$$

The absolute value of this function is again 1. The presence of the resonant frequency ω_r is explained by the fact that this function concerns a resonant circuit. This frequency may be calculated from

$$\omega_r = \sqrt{\alpha^2 + \beta^2}$$

in which α and β are the poles of the function.

The Q factor is

$$Q = \omega_r / 2\alpha.$$

The phase shift of a second-order filter is

$$\varphi = -2\arctan\frac{\omega\omega_r}{Q(\omega_r^2 - \omega^2)}$$

while the time delay is calculated from

$$t = \frac{2\omega_r^2(\omega_r^2 + \omega^2)}{Q(\omega^2 - \omega_r^2) + \frac{\omega^2\omega_r^2}{Q}}$$

From these formulas, it is clear that the computations of a second-order network are not all that simple. The time delay is largest at the resonant frequency. The higher the Q, the more pronounced the peak in the time delay characteristic.

Practical passive networks

The design of a first-order delay network is fairly simple. Fig. 52 shows two possibilities: a ladder type and an asymmetric type. Both filters have identical output

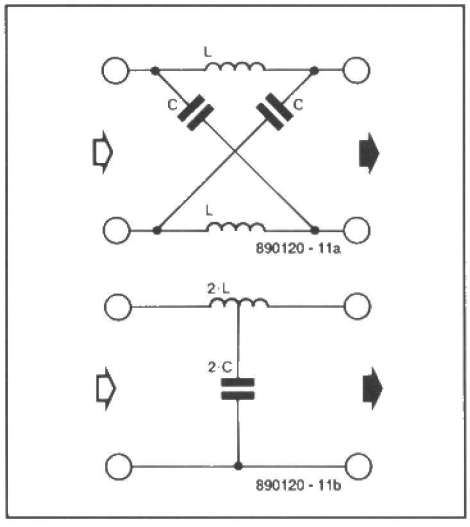


Fig. 52. First-order delay networks: (a) ladder type; (b) asymmetric type.

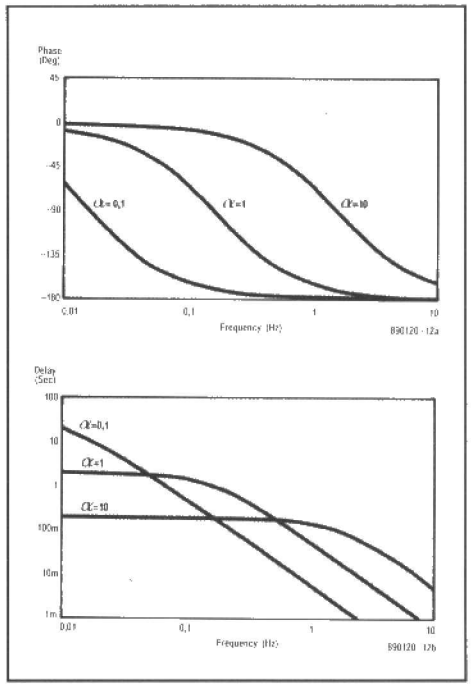


Fig. 53. Time delays of a first-order network at α-values of 0.1, 1.0 and 10 respectively. Fig. 2a shows the phase shift and 2b the time delay.

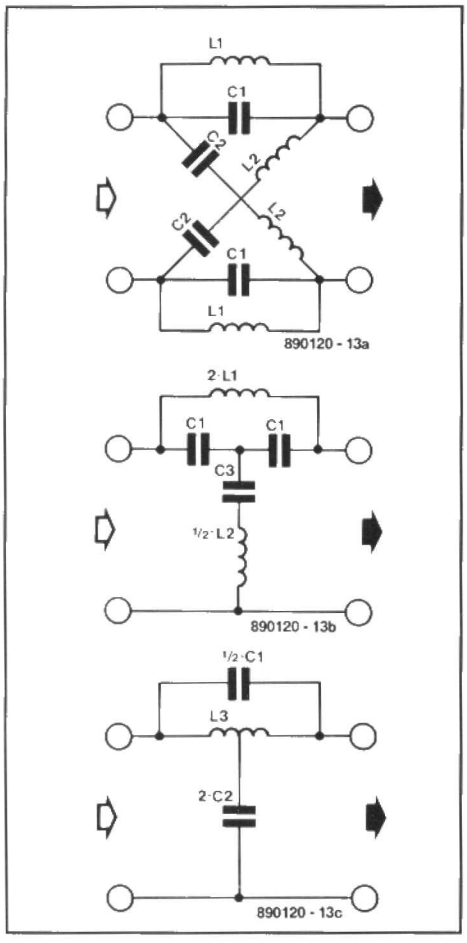


Fig. 54. Circuit diagrams of (a) a second-order ladder network; (b) an unbalanced network with a $Q > 1$; and (c) an unbalanced network with a $Q < 1$

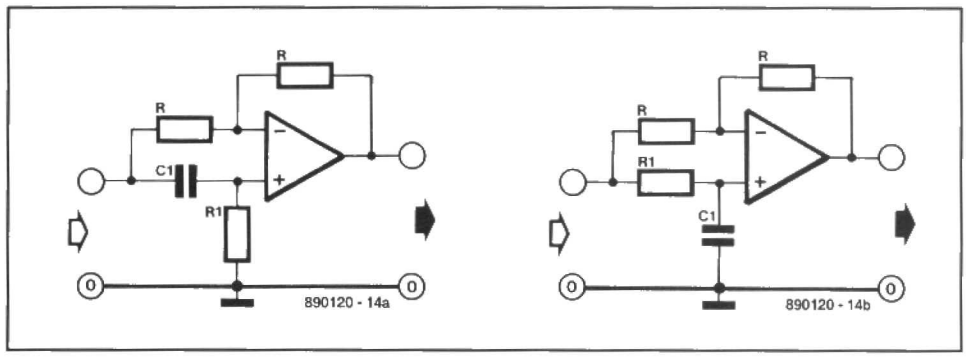


Fig. 55. Designs of active first-order networks: 55a shows a lagging network and 55b a leading one.

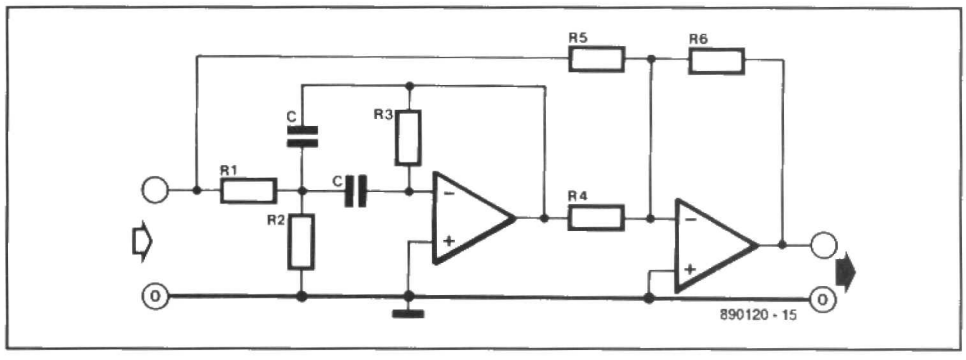


Fig. 56. An active second-order network; this design is suitable for Q-values from 0 to 20.

impedances, so that they may be cascaded without any problems. The compuation of such a filter is quite easy:

$$L = R / \alpha$$

$$C = 1/\alpha R$$

where R is the desired output impedance.

The construction of the ladder network should not present any difficulties, but in building an asymmetric type it should be borne in mind that the inductor is centre-tapped: the magnetic coupling factor between the two halves must be 1.

The phase shift and time delay curves given in Fig. 53 are given for a-values of 0.1, 1.0 and 10. Note that the value of a may be chosen freely, dependent, of course, on the desired time delay curve.

Second-order networks are a little more complicated and may be designed for Q-values smaller and greater than 1. Several designs are shown in Fig. 54: in (a) a ladder network; in (b) an unbalanced filter for Q-values greater than 1 and in (c) an unbalanced filter for Q-values smaller than 1. The designs in (a) and (b) use standard components throughout, whereas that in (c) requires a centre-tapped inductor. The values of the various components are calculated as follows.

$$L_1 = \frac{2\alpha R}{\alpha^2 + \beta^2}$$

$$C_1 = \frac{1}{2\alpha R}$$

$$L_2 = \frac{R}{2\alpha}$$

$$C_2 = \frac{2\alpha}{R(\alpha^2 + \beta^2)}$$

$$L_3 = \frac{R}{\alpha} + \frac{4\alpha R}{\alpha^2 + \beta^2}$$

$$C_3 = \frac{4\alpha}{R(\beta^2 - 3\alpha^2)}$$

Active networks

There are even better possibilities of designing active all-pass networks than passive ones, but for clarity's sake they will be restricted to first- and second-order networks.

Good designs of a first-order filter are shown in Fig. 55: (a) is an inductive type and (b) a capacitive type. Furthermore, both circuits invert the input signal (which has nothing to do with the phase shift). Note that not a few people mix up the two circuits under the impression that the one in (b) is a lagging type.

The components in these circuits are calculated as follows.

$$\alpha = \frac{1}{R_1 C_1}$$

$$t_{DC} = 2R_1 C_1$$

$$t = \frac{2R_1 C_1}{(\omega R_1 C_1)^2 + 1}$$

$$\varphi = -2\arctan(\omega R_1 C_1)$$

The design of an active second-order network is shown in Fig. 56. It consists of a band-pass filter and a summing amplifier. The computation of the components is rather more complicated than with the first-order filter. First we assign a value to C and then:

$$R_1 = R_3/2$$

$$R_2 = \frac{R_1}{2Q^2 - 1}$$

$$R_3 = \frac{1}{\alpha C}$$

Next, $R5$ is given a suitable value, say, 22 kΩ. For unity gain, $R6 = R5$, but if amplification is required, $R6$ should be given a larger value.

For Q-values greater than 0.7, $R2$ is not required, while

$$R_1 = R_3/4Q^2$$

and

$$R_4 = R_5 Q^2$$

With the aid of second-order all-pass networks, it is possible to design delay lines that have a constant time delay over a given range of frequencies. The pole positions may be obtained from the tables given earlier in the series. The calculations are fairly complicated and will not be gone into here.

Although it is possible to design delay lines in this manner, the normally specific requirements of these devices make it difficult to to give general examples. The formulas given in this final part must, therefore, suffice.

NEW BOOKS

European Scrambling Systems: Circuits, Tactics and Techniques
by J.W.A. McCormac
270 pages – 210 × 148 mm
Price £29.00

Books on Satellite TV are hard to find in most bookshops, but J. Vincent Technical Books can supply a whole range. *European Scrambling Systems* is one of their latest and is aimed at educational establishment and the experimentalist.

The book deals with scrambling and unscrambling methods from the simple to the MAC system and Eurocrypt and as such is indispensable reading for all interested in the encryption of video and audio signals used in broadcasting and cable systems.

J. Vincent Technical Books • 24 River Gardens • Purley • READING RG8 8BX • Telephone (0734) 414468.

The DOS 3.3 and OS/2 Handbook
by Stephen Morris
ISBN 0 434 91284 0
352 pages – 245 × 190 mm
Price £ 19.95

DOS 3.3 , the latest member of the family of operating systems for the IBM PC and compatibles, and OS/2 are the two alternative systems that can be used with the PS/2 series of computers. Since they are so similar, most of the text of the book applies to both operating systems. Any new features of OS/2 are covered in their own separate sections.

The handbook, aimed at both the new user and the experienced operator, is divided into four parts.

Part 1 is intended for the new user, introducing the concepts and basic structure of the two operating systems.

Part 2 describes the full command set, so that the experienced operator can tailor the system to his own particular requirements. It includes a number of worked examples.

Part 3 covers batch files and their use, from simple files for the new user to full batch-file programming.

Part 4 goes deeper into the heart of the operating systems and covers, briefly, the way in which they work and how more use may be made of their advanced functions within programs.

Audio IC Circuits Manual
by R.M. Marston
ISBN 0 434 91210 7
168 pages – 215 × 136 mm
Price £ 11.95

This manual, the fourth by R.M. Marston in a new series of practical circuits manuals, is a guide to the vast range of audio and audio-associated ICs that is now readily available for use by amateur and professional design engineers and technicians. Including over 240 diagrams, it deals with LF linear amplifiers, dual preamplifiers, AF power amplifiers, charge-coupled device delay lines, bar-graph display drivers and power supply regulators, and shows how to use these devices in circuits ranging from simple signal conditioners and filters to complex graphic equalizers, stereo amplifiers systems, and echo/reverb delay line systems.

The book should be of particular interest to the practical design engineer, technician and the experimenter, as well as the electronics student and amateur.

Heinemann Professional Publishing • Halley Court • Jordan Hill • OXFORD OX2 8EJ.

Computers and Music: an Introduction
by R.A. Penfold
ISBN 1 870775 07 4
174 pages – 215 × 137 mm
Price £7.95

Early attempts at getting computers to produce music were of limited success, but now they are playing an increasingly important part in the world of music. In fact, some modern electronic instruments can produce excellent music without any external assistance.

However, even with the 'user friendliness' of modern computers, the prospective computer music user has a number of hurdles to overcome. This book will help you learn the basics of computing, running application programs, wiring up a MIDI system and choosing the right components for a system to suit your personal needs, as well as equipping you to use that system to the full.

PC Publishing • 4 Brook Street • TONBRIDGE TN9 2PJ • Telephone (0732) 770893

Controlling with Computers
by John Billingsley
ISBN 0 07084 193 4
296 pages – 228 × 152 mm
Price £11.95

Books on control theory can not be easy, but they are invariably fascinating and *Controlling with Computers* is no exception. It presents a course in control theory in an accessible and progressive manner, leading to an understanding of advanced methods for practical computer control.

The computer plays a large part in appreciating the material covered in the book. With the aid of a few lines of software and a PC, the reader can simulate dynamic systems in real time. Other programs, small enough to type into the machine within a few minutes, give access to on-screen graphical analysis, including Bode, Nyquist, Nichols and Root Locus in both s and z planes.

Apart from these, the text covers modelling and simulation, matrix state equations, feedback and stability analysis by matrix methods, software implementation of filters, practical computer control, nonlinear control and optimization.

Mathematical topics are included in 'preludes' to the chapters in which they are needed and include matrix analysis, complex functions and mappings, Fourier, Laplace and z-transforms, and convolution.

Throughtout the text there are worked examples, problems and solutions to lead the reader to a thorough working knowledge of control principles and techniques.

McGraw-Hill Book Company (UK) Ltd Shoppenhangers Road • MAIDENHEAD SL6 2QL.

INTRUDER ALARM

In today's society, it makes good sense to provide some form of intruder alarm system in the home, if for no other reason than the family's peace of mind. Effective, reliable and simple to control, the intruder alarm system described in this month's article uses readily available low-cost components only.

E. Chicken, MBE, BSc, MSc, CEng, FIEE

Apart from its low current demand from a battery during non-alarm conditions, the alarm is also noteworthy for its system-test bleep on switching on and on leaving the house, its pulse drive of the external sounder to economize on battery power, and automatic time-out of the internal and external sounder to minimize social disturbance.

The block diagram given in Fig. 1 shows the various stages of the circuit, their interconnections and related signal routes. The way in which the stages interact in detail is explained below.

Circuit description

Power supply

As shown in the circuit diagram of Fig. 2, the alarm is powered by a small 12 V rechargeable battery that is trickle-charged by a mains adapter with d.c. output. In the quiescent condition, the current drain from the battery is less than 1 mA. Current consumption in the actuated condition is virtually that of the external sounders alone. Charging current for the rechargeable battery is limited to about 15 mA by R_7 in series with LED D_4, which, mounted on to the front-panel of the enclosure, serves as a charging indicator. The output voltage of the mains adapter must be measured and the value of R_7 chosen such that the maximum LED current of about 20 mA is not exceeded.

On/off control

Control of the alarm system is effected by a single-pole ON/OFF switch, S_1. Actually, the circuit is never switched off completely as long as the battery is connected, but the current drawn with the switch in the OFF position is negligible.

Closing S_1 to switch the system off connects R_2 to the negative supply rail, causing T_1 to conduct. Diode D_1 is forward-biased, and the resultant voltage drop of about 0.6 V maintains conduction of T_1 in the event of a reduction of the supply voltage. That conduction in turn maintains the off condition of the system, and so minimizes the possibility of false alarms.

When T_1 is switched on, D_3 ceases to conduct so that C_1 is charged to the supply voltage via R_5 and R_6. For convenience, low voltages from 0 to, say, +2 V will be referred to as logic 0, and the higher +12 V supply rail voltage as logic 1.

This voltage on C_1 forms a logic 1 that is inverted by NAND gate N_1 to present a 0 to one of the two control inputs of the bistable formed by N_2 and N_3. So long as pin 6 of N_2 remains at 0, the output of the bistable, pin 4 of N_2, is held at 1 to prevent the alarm sounders being actuated.

Switching the system off simultaneously takes the RESET pins of timers IC_2 and IC_3 low, which prevents the timers being inadvertently triggered into a false alarm sequence. As long as the system is switched off, D_2 is forward-biased via T_1 and R_{14}.

When the system is switched on, switch S_1 is in fact opened, so that T_1 ceases to conduct. This causes the collector voltage to drop to practically 0 V via R_4, so that D_3 is forward-biased via R_5 and R_4. As a result, C_3 discharges slowly via R_6, D_3 and R_4. The lowest voltage on C_3 is reached in about 15 seconds, determined by time constant $C_1(R_4+R_6)$.

The final voltage on C_1 as determined

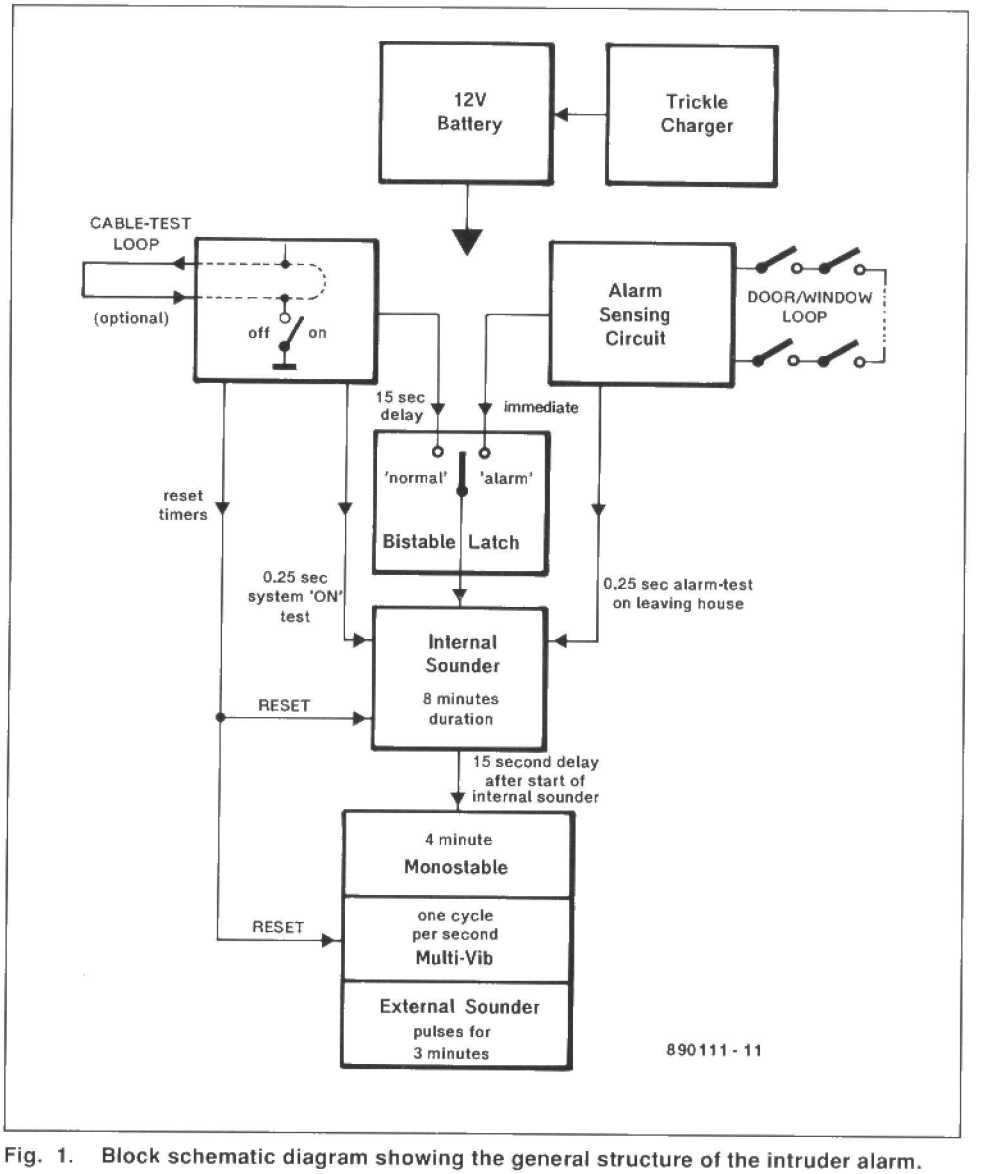


Fig. 1. Block schematic diagram showing the general structure of the intruder alarm.

by potential divider R_5-R_4 is about one tenth of the supply voltage, plus the forward drop of D_4. In total, this makes about +1.8 V, which represents a logic 0. The resultant logic 1 at the output of NAND gate N_1 causes bistable N_2-N_3 to toggle 15 seconds after switching the system on. The logic state at output pin 4 of the bistable becomes 1, and can be changed to 0 according to the logic level applied to the control input terminal, pin 1 of N_3.

Alarm sensing

When all doors and windows protected by the detector loop are closed, and assuming that the detector switches are of the normally-closed type, R_{13} is connected to the negative supply rail, causing T_2 to conduct via R_{12}-D_7-R_{13}. The function of D_7 is similar to that of D_1 as discussed earlier. With all detector switches closed and the loop unbroken, D_6 conducts via T_2 and R_{14}. Diode D_5 does not conduct because its cathode is connected to the positive supply rail via T_2, as is its anode via R_8.

Capacitor C_3 supplies a logic 1 to the second input of bistable N_2-N_3 after it has been charged via R_8 and R_9. The two logic 1s at the bistable inputs maintain a 1 at the output, pin 4 of N_2. As stated earlier, this 1 inhibits the sounding of an alarm.

Breaking the detector loop disconnects R_{13} from the negative supply rail, causing T_2 to stop conducting. Its collector potential drops to nearly 0 V, so that D_5 is forward-biased via R_8 and R_{10}. As a result, C_3 discharges in about 0.5 s via R_5, D_5 and R_{10}, its terminal voltage dropping to about +1.8 V, which represents a 0.

The 0.5 s delay produced by C_3-(R_9+R_{10}) assists in the prevention of false alarms by interference spikes and other transients in the loop circuit such as by doors shaking in the wind.

Control terminal pin 1 of the bistable accordingly changes from 1 to 0, so that the level at the output terminal changes from 1 to 0, where it will remain latched in the absence of an alarm condition until the other control terminal, pin 6 of N_2, changes state, i.e., until the system is switched off. The condition necessary for the generation of alarm signals is a 0 at the output of the bistable.

Sounder timing

The alarm system has provision for two sounders, one low-power internal alarm such as an active piezo-electric buzzer, and one high-volume external alarm such as a 12 V bell.

The circuit automatically switches off each of the alarm sounders after a reasonable period of time: 4 minutes for the external sounder, and 8 minutes for the internal sounder. The individual timing circuits may be altered, however, to suit personal preference.

Low-power CMOS timers Type 555 (IC_2) and 556 (IC_3) are used in the interest of battery economy. When the circuit is switched on, the timers are simultaneously released from the reset condition because their pins 4 are taken logic high.

Internal sounder

While the system is on, any break in the detector loop, such as by a protected door or window opening for longer than 0.5 s, initiates operation of the internal sounder. When the loop is broken, C_6 passes the 1-to-0 transition at the output of the bistable to pin 2 of IC_2, which is triggered into monostable operation for a period of about 8 minutes. Network C_6-R_{16} forms a differentiator to sharpen the trigger pulse.

On entering the premises, residents have about 15 s to switch off the system before the monostable switches on the internal sounder. Prior to the arrival of the trigger pulse at pin 2 of MMV IC_2, its output, pin 3, is normally at 0. This level keeps T_4 off via base resistor R_{19}. Immediately upon the arrival of the negative-going trigger pulse at pin 2 of IC_2, its output rises from 0 to 1. This level is maintained for about 8 minutes as determined by C_8-R_{17}. Transistor T_4 is switched on, and actuates the internal sounder in its collector circuit. When the 8-minute period has lapsed, the low level at pin 3 of IC_2 causes the internal sounder to be turned off by T_4.

For convenience of testing during the construction and installation stages, LED D_9 provides a visual indication of circuit operation without the internal sounder being connected. If actuated, the internal sounder is switched off simultaneously with the system.

External sounder

The operation of the external sounder circuit is slightly different from that of the

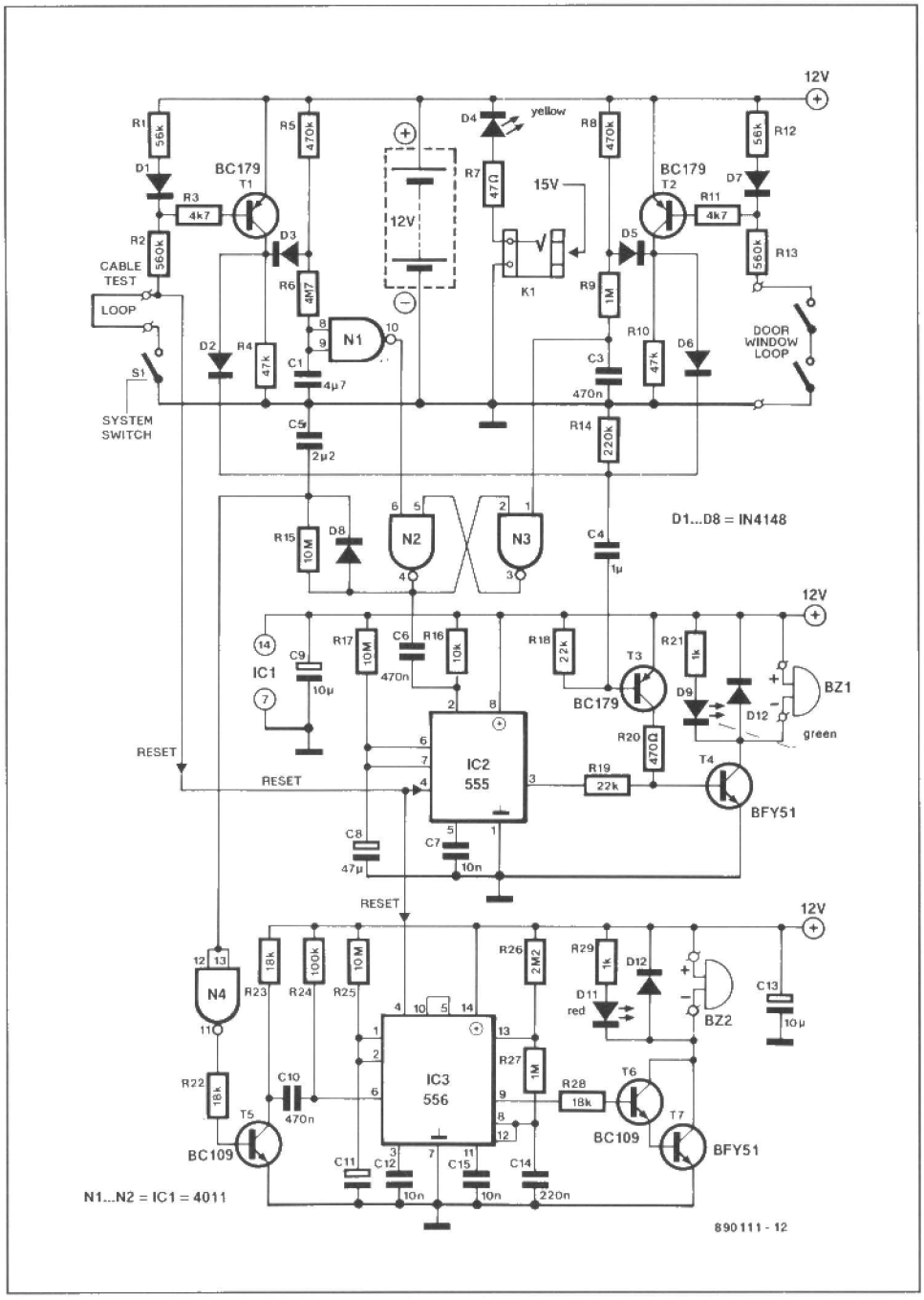


Fig. 2. Circuit diagram of the intruder alarm. Note that the timers, IC2 and IC3, must be low-power versions to ensure minimum current drain from the battery.

internal sounder. Assuming that the system is switched on and the detector loop not yet broken, the output of bistable N_2-N_3 is at 1. Capacitor C_5 charges rapidly via D_8, until its terminal voltage is also at 1. Subsequently, T_5 is turned off by the 0 supplied by inverter N_4. Timer IC_3 is not yet triggered into action, so its output terminal, pin 9, is at 0. Hence, darlington transistor T_6-T_7 is kept off in the absence of an alarm signal — external sounder Bz_2 is not actuated.

Circuit IC_3, a CMOS Type 556, contains two timers Type 555. Pin 4 of the first 555 in the chip is held logic high via R_2-D_1-R_1, so the timer is ready to be triggered. The instant the detector loop is broken, the 1-to-0 pulse transition at the output of bistable N_2-N_3 causes D_8 to block, enabling C_5 to discharge through R_{15}. The time constant formed by these two components introduces a delay of about 15 s in the transition from 1 to 0 at the input to inverter N_4. After this delay, the resultant transition from 0 to 1 at the base of T_5 causes the transistor to conduct. The collector voltage of T_5 drops from 1 to 0, and the negative-going pulse edge is differentiated by C_{10}-R_{24} to be passed as a sharpened trigger pulse to pin 6 of dual timer IC_3. The first timer in IC_3 is configured as a monostable with a 4-minute time period, the output of which is used to control the second timer circuit, which is configured as an astable multivibrator (AMV). This circuit can produce its 1-s on/off pulse rate only during the 4-minute period of operation set by C_{11}-R_{25} for the preceding monostable in the IC. The time period, t, in seconds can be calculated from

$$t = 1.1(C_{11}R_{25})$$

Output pin 5 of the first timer is normally at 0 until the arrival of an input trigger pulse, whereupon the output state changes abruptly from 0 to 1. Pin 5 is wired to the reset input, pin 10, of the second timer in the IC package. When taken high, this pin enables the AMV to oscillate at a rate of 1 Hz during the 4-minute period defined by the first timer. The period (in seconds) of the oscillator signal is calculated from

$$t = 0.7C_{14}(R_{26} + 2R_{27})$$

The square-wave oscillator signal drives darlington transistor pair T_6-T_7, so that the external sounder, Bz_2, is switched on and off at a rate of about 1 s until the 4-minute monostable period has lapsed. As with the internal sounder, a visual indication of external alarm activity is provided. Diode D_{12} protects T_7 from transient voltage spikes generated as the current through the inductance formed by Bz_2 is interrupted. Capacitors C_{12} and C_{15} are for decoupling and do not form part of the timing circuits.

System assurance bleep

Provision has been made for a system assurance bleep to indicate that the system is functional, prior to the resident's departure from the premises. Two assurance bleeps are generated: one before the end of the 15-s switch-on delay at the instant of switch-on, and one as the exit door is opened for departure.

While the system is switched off, C_4 has no voltage on it because T_1 conducts. Following switch-on, the 15-s delay before the system becomes 'live' allows time for the injection of a short control signal direct to the internal sounder control transistor, T_4, bypassing timer IC_2.

When the circuit is switched on, T_2 and D_2 become non-conductive so that C_4 is allowed to charge via R_{18} and R_{14} in about 0.25 s, which in effect momentarily causes the base of T_3 to be taken low via R_{14}. The upshot is that both T_3 and T_4 conduct just long enough to enable the internal sounder to produce a short bleep.

The same process occurs with T_2 and D_6 which, like D_2, is connected to the junction of C_4 and R_{14}, except that in this case the charging of C_4 is initiated by the breaking of the detector loop when a protected door or window is opened.

Construction

A convenient and low-cost method of construction is to use readily available copper SRBP stripboard with 0.1-inch hole spacing. The use of sockets for the ICs is recommended, but the layout of components is not at all critical.

Inter-component wiring is by thin insulated wire. If stranded wire is used, care must be taken to avoid unintended contacts by loose unsoldered strands.

The external wires are connected to terminal posts on the board. The two alarm-test LEDs are purposely located on the board for visual access during testing.

A separate box may be required to accommodate the battery, and possibly the mains adapter.

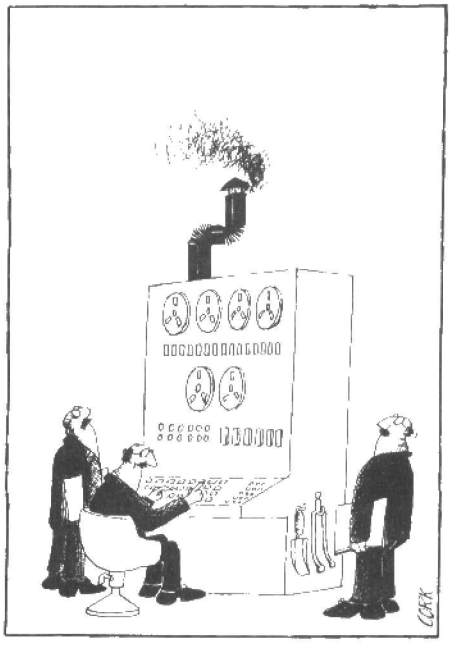
The ON/OFF switch is either a key-operated type, or a cheaper standard on/off miniature toggle switch. A reasonable compromise as regards safety might be to use a standard SPST toggle switch, and to conceal it from view either complete with the electronic assembly, or in a small separate enclosure.

Further practical considerations

The door and window switches are magnetically operated types that have the advantage of not drawing current from the battery. Constructors wishing to include a motion detector of some sort in the loop must bear in mind that such a device may well draw 20 mA or more whether actuated or not, which would have to be taken into consideration when choosing the battery and the associated charger. Also, the motion detector requires a separate cable to carry its supply voltage. One approach might be to replace the single-pole on/off switch with a double-pole (DPDT) type, the other pole of which is used to connect the +12 V to the motion detector only while the system is switched on, assuming that the battery is being recharged during the off condition.

The cable-test loop shown in the circuit diagram provides an indication in the event of the loop having been tampered with, for instance, cut by a prospective intruder who plans a return visit while the house is unoccupied. It would need to be a separate pair but within a two-pair cable; if both pairs are cut simultaneously, the system would be switched on, and the detector loop to be broken, so that the alarm is set off immediately. If such a situation is thought unlikely, the cable-test loop may be omitted, and a substitute wire link installed on the board. The detector loop would then need to be twin PVC insulated cable of, say, 7×0.2 mm running from the board to each detector in turn, and back to the board via the unbroken wire of the pair.

The choice of the external sounder is entirely up to the constructor, but care should be taken not to overload the transistor driver or the battery. The author used a weatherproofed sounder giving a choice of continuous or warbling tone at a sound level of 107 dBA for only 20 mA of current drain from the 12 V battery. It is standard practice to enclose the external sounder in a weatherproof enclosure, installed high up on the wall out of easy reach, and with its supply cable hidden behind the box as an anti-tamper precaution.



DESIGN IDEAS

The contents of this column are based solely on information supplied by the author and do not imply practical experience by *Elektor Electronics*.

PROTECTING ASYNCHRONOUS MOTORS

by Mehrdad Rostami, University of Tehran, Iran

The circuit described here was designed for protecting heavy-duty asynchronous motors during the start-up period. As is well-known, without protection such motors may easily get damaged by poor starting. The circuit may also be used for other applications where a trip circuit needs to be triggered, such as, for instance, in the monitoring of liquid levels.

Every motor has a time-speed characteristic that shows how, or otherwise, it starts and reaches its normal speed. A number of such curves are illustrated in Fig. 1. If the characteristic of a particular motor is similar to the lower (bold) one, any attempt at starting the motor should be stopped immediately and the motor in-spected thoroughly. The dashed curve in-dicates the lower limits of acceptable motor performance, while the upper curve shows normal values of a properly functioning motor.

Circuit description

The circuit diagram in Fig. 4 consists of five identifiable blocks: (1) oscillator and time base—IC4, IC5 and IC6; (2) address unit and memory—IC7, IC8 and IC9; (3) shaft pulse receiver and counter—IC14 and IC15; (4)comparator—IC12 and IC13; and (5) automatic stop unit—FF1 and FF2.

The input to the circuit consists of pulses generated by a rotary encoder comprising an opto-coupler and perforated man-made fibre disk fitted securely on to the shaft of the motor as shown in Fig. 2. The pulses generated by the opto-coupler are applied to receiver/counter IC14 and then to counter IC15.

The 555 oscillator,. IC4, generates 50 Hz pulses that are divided by 5 in IC5. The output of this IC is taken to switch S1 and also applied to a second :5 divider, IC6.

The output of either divider may be selected by S1 and from there applied to cascaded circuits IC9 and IC10. The output of IC10 is used to reset the shaft pulse counters, IC14 and IC15, at the end of each period of 0.5 s or 0.1 s depending on the setting of S1, and also to clock the address unit, IC7 and IC8.

The EPROM must be loaded with the data of the appropriate motor curve. If, for instyance, the rotary encoder is supposed to send eight pulses in the first 0.5 s period (S1 set to 2 Hz)—which, of course, depends not only on the rotary speed of the shaft of the motor, but also on the number of perforations in the disk—the first memory cell of IC11 must be loaded with 00001000. The number of pulses is determined from the timing diagram of the relevant motor: a typical ttime vs rotary speed characteristic is shown in Fig. 3.

Similarly, if the pulse generator is supposed to send 12 pulses in the second 0.5 s period (S1 set to 2Hz), the second memory cell of the EPROM must be loaded with 00001100. This process must be repeated for each subsequent 0.5 s period (up to a total of 20 seconds, when a properly working motor will have started).

The outputs of the EPROM and the shaft pulse counters are applied to two Type 7485 comparators, IC12 and IC13.

At the end of each 0.5 s period, IC9 generates a pulse that is used to drive one of the inputs of AND gate N2 high. When the level at pin 7 of comparator IC13 is also high, the second input of N2 goes high.also. This results in the output of this gate becoming a logic 1, which is applied tots of AND gate N3.

The second input of N3 is supplied by AUTOSTOP unit FF1, a D-type bistable. This bistable is reset by AND gate N1 when address 00010100 is applied to the EPROM. Its Q output then goes high, which causes the second input, and thus the output, of gate N3 to go high. This causes a second D-type bistable, FF2, to be set. When that happens, the coil of a trip device in the starting circuit of the motor is energized so that the starting circuit is broken.

Circuits IC12 and IC13 compare the data input from the EPROM with that from counters IC14 and IC15. If these data streams are identical, pin 7 of IC13 re-mains low, preventing the operation of the automatic stop unit.

Schmitt triggers N4, N5 and N6 form an auto reset circuit for setting/resetting the bistables and returning the counters to their original state.

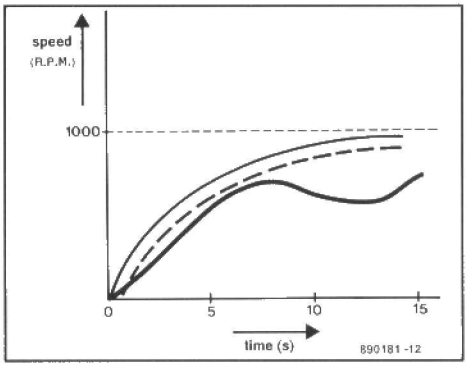


Fig. 1. Time-speed characteristics of a an asynchronous motor. The lower (bold) curve indicates a defect motor; the dashed curve indicates the lower limit of acceptable performance; and the upper curve is typical for a properly functioning motor.

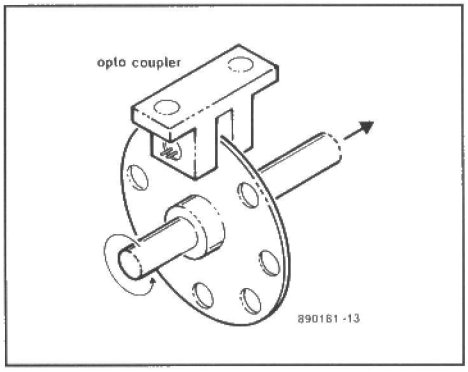


Fig. 2. The rotary encoder consists of an opto-coupler and a perforated man-made fibre disk fitted on to the shaft of the motor

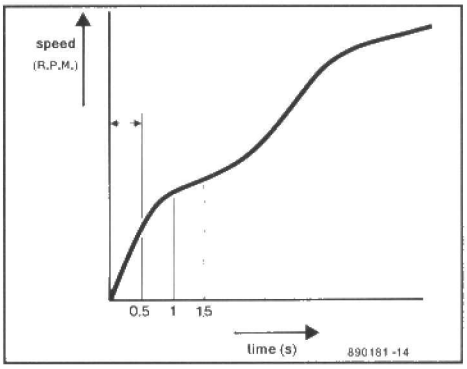


Fig. 3. Typical time vs rotary speed diagram of an asynchronous motor. A properly working motor should start within 20 seconds.

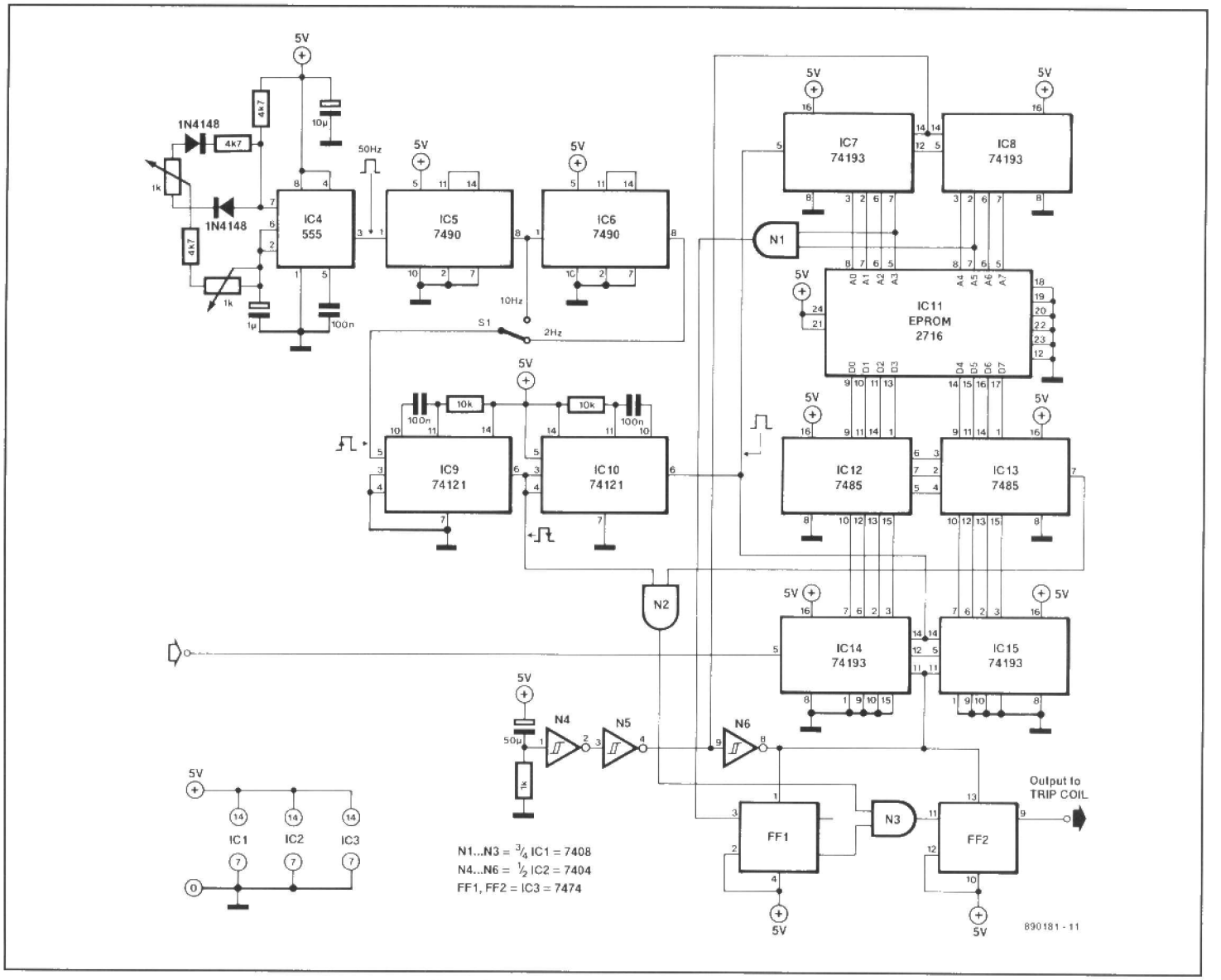


Fig. 4. Circuit diagram of the protection unit.

IEE Meetings

2 Nov — Measurements and modelling of microwave devices and circuits.
6 Nov — Algorithmic and knowledge based CADS for VLSI.
7 Nov — Influenece of room acoustics on reproduced sound.
8–10 Nov — Computers and safety (Cardiff).
9 Nov — Television automation: today's technology, tomorrow's opportunities.
13 Nov — Transputer applications.
13 Nov — DBS playout centre.
14 Nov — Advanced manufacturing in electronics: education and training implications.
16 Nov — Hold on to your engineers.
17 Nov — User interface management systems.
17 Nov — Computer integrated test and manufacturing.
22 Nov — National debate: the electrical engineer's commitment to safety and to the environment.

EVENTS

23 Nov — Milestones in telecommunications.
27 Nov — New directions in VLSI design.
27 Nov — Is BS5750 relevant for quality software?
28 Nov — Circuits and devices for data communications.
28–30 Nov — Satellite communications (Munich).
29 Nov — Navigation, guidance and control in aerospace.
30 Nov — Specification of complex systems.

Further information on these, and many other, events from IEE • Savoy Place • LONDON WC2R 0BL • Telephone 01-240 1871

COMPEC, the Computer Peripherals Exhibition and Conference will be held at Olympia, London, from 14 to 17 November. Details from Cahners Exhibitions Ltd Chatsworth House • 59 London Road TWICKENHAM TW1 3SZ • Telephone 01-891 5051.

The **Coil Winding International Exhibition and Conference** will be held at the National Exhibition Centre, Birmingham, from 14 to 16 November. Details from Evan Steadman (Services) Ltd • The Hub • Emson Close • SAFFRON WALDEN CB10 1HL • Telephone (0799) 26699.

Techmart, the Technology Transfer Exhibition will be held at the National Exhibition Centre, Birmingham, from 15 to 17 November. Details from Focus Events Ltd Greencoat House • Francis St • LONDON SW1P 1DG • Telephone 01-834 1717.

SCIENCE & TECHNOLOGY

Intelligence, Intentionality and Self Awareness

by Dr T. Farrimond, University of Waikato, New Zealand

This paper deals with some of the problems in ascribing intelligence to computers. It is suggested that machines which only process the symbols of language are not intelligent even though they may produce an output similar to that from an intelligent human. It is maintained that self awareness in humans, coupled with the ability to interact directly with the environment by means of the senses, is central to intelligent functioning, which includes the development of a social/ecological conscience.

In his article "Artificial Intelligence", M. Seymour[1] provides an interesting and informative account of some of the problems met by computer designers in attempting to produce machines that exhibit artificial intelligence. The article discusses arguments for and against what constitutes artificial intelligence including the existence or otherwise of intentionality (Searle, 1984)[2]. The present paper examines some of the concepts from the point of view of a psychologist, who was a student at Manchester when Alan Turing was working on the theoretical aspects of information processing. The power of electronic devices has increased enormously since that time, but perhaps there has not been a similar growth in defining the terminology used to describe computer activities and brain activities.

At the simplest level there has been revival of anthropomorphism, a condemnatory appellation feared by biologists accused of reading human characteristics into the behaviour pattern of lower animals. However, equally imprecise use of language is exemplified by phrases such as 'computers talking to each other'. This is largely a matter of economy in the use of words, since it is easier to use concepts already in existence than to invent new ones, but there are dangers in over-extending the concepts to include things that are not justifiable. The problem is that with terms such as intentionality it is difficult to provide a definition that does not also include or imply the term intention, which then also has to be defined. In describing a spiral staircase, it is easier to make a visual representation by drawing one (or to wave one's arm to illustrate the concept) than it is to describe it verbally. If this is true for a concrete example such as this, then for abstract concepts the difficulties involved in using words to define them are enormous.

Is the term intentionality sufficient to cover those things the brain does that are different from a computer? How does one recognize intentionality? Can intentionality be proven and is it important to do so? The concept of intentionality is essential in dealing with human affairs, particularly when legal disputes arise and require resolution. We resort to a court of law where proof of intention may well determine the outcome of a case. Did the accused know what she was doing when she set fire to her husband's bed? Evidence may be produced to prove diminished responsibility; a person may be described as intellectually sub-normal and so not accountable for his/her actions. The implications in this case may be that the accused did not properly understand that the outcome of the action might be injury or death. Similar incapacity may also be ascribed to a person under the influence of drugs or suffering from some mental disorder. The question of responsibility is the key to determining whether the sentence should be 10 years or alternatively some form of medical treatment. In each case what is examined are the following.

(a) Could the individual predict the outcome of the act that caused the accident (is there an ability to follow a logical sequence of events on a probabilistic basis to a conclusion or variety of possible conclusions)?

(b) Did the person **intend** to set in train the causal events that resulted in harm? If a person accidentally backs into a lever that releases a winch carrying a load of iron, causing it to fall and kill someone it is not the ability to understand the causal relationships that determines guilt – but whether there was **intention** to do harm. In this example there was not.

(c) Was there an **awareness** on the part of the accused that he or she was carrying out the action?

Point (c) is relevant, for example, in the case of hypnosis. A woman under hypnosis may be persuaded to role-play the part of someone in authority and perform an act not normally acceptable to her simply because she regarded herself as another person during the period of hypnosis. In this case a **causal** sequence of events has occurred in which there is **intention** on the part of the subject to carry out an act, but because self awareness is absent, the individual would not be regarded as culpable in law. Even though her behaviour incorporates the two elements usually considered necessary for intelligent behaviour, i.e., it exhibits appreciation of **causality** and also **intentionality**, she is not seen as responsible for her behaviour. It may be argued that intelligent human behaviour involves these elements – causality, intention and self awareness and for a computer to be regarded as intelligent it also should exhibit the same properties.

It is this point of self awareness which I contend is different from intentionality and is possibly the central issue in determining whether behaviour is intelligent or not. It is assumed that the use of the term intelligence is a reference to human mental and behavioural processes since these are the only points of reference we have for what we mean by intelligent behaviour.

External behaviour

Would a machine designed to look and move exactly like a human being so that it would

be accepted at a barbecue (or even a social function!) really be intelligent? One could forgive the hostess for assuming that it is, since from the outside the machine does all the things normally expected of a human: it speaks, moves about, listens attentively and even laughs in the appropriate places.

It is tempting to argue that it is only the behaviour of the machine that is important, i.e., outside appearances and behaviour are all that matter. If these are indistinguishable from human behaviour, the machine should be regarded as human, and therefore intelligent. Indeed, this may be the effect on the hostess until it is demonstrated to her that a group of electronics enthusiasts have constructed the machine and are operating it remotely: one controlling locomotion, another speech, and so on. Thereafter, the hostess would no longer accept as fact that because someone (thing) exhibits intelligent human behaviour it is genuinely intelligent. This emphasizes the problem that without further knowledge about the controlling mechanisms it is difficult to prove that a behaviour pattern is intelligent or not. But is is obviously not safe to infer intelligence on behaviour alone. In the example given, the intelligence is elsewhere and is external to the machine.

A distinction should be made between the analogous behaviour and identical behaviour. Herein lies the distinction between machines at present and humans. The behaviour of a machine may be analogous to that of a human without necessarily being identical.

Although it may be the expressed aim of engineers to produce intelligent machines, it is doubtful whether they would want them to be intelligent in the human sense, since they may no longer wish to co-operate with the inventor – and may prefer to go on strike. Certainly, any organism (biological or mechanical) with self awareness would also be aware of its rights as a thinking being and its utility as a tool (that is, slave) would be reduced. An interesting prospect also opens up in the area of culpability for mistakes. If a machine is regarded as culpable and it transgresses, what should its punishment be?

Absence of need for programming

It has been envisaged that one day it may be possible to build a machine that can think, that is, need not be programmed to perform its functions. This statement as it stands perhaps needs elaboration before its implications can be considered. If the term 'thinks' refers to performing certain analytical functions, the similarity to human thinking is restricted to one level of activity. It would be necessary to define the term in other ways if it were to include intentionality and self awareness. The presence of one level of functioning does not automatically mean that the other levels are present. Terms such as intelligence, cognition, perception, etc., have evolved from attempts to categorize (by using symbols) certain aspects of human behaviour. The words are not specific but incorporate implied connections with all other aspects of human mental activity.

Gregory in his book *The Intelligent Eye* emphasizes the relationships that exist between the eye and the brain. The eye is an extension of the brain in a psychological as well as in an anatomical sense. The unitary nature of perception, cognition, intelligence, etc., makes it difficult to talk about simply one aspect of human behaviour without automatically including all the others. It would make little sense to examine human cognition without at the same time considering intelligence, memory store, and perceptual abilities, for cognition depends upon them all. Also, an individual's cognitive state is constantly changing, not only from new experiences, but by re-analysis of stored information from within, where models exist of the world (imagery) available to the individual for the process of thinking, researching and creating.

The capacity of the brain

In an attempt to duplicate the equivalent of a neural net system as found in the brain, experimenters have constructed electronic networks with a large number of interconnections. However, the human brain is not simply a neural network. The complex of 10 billion (10^9) interconnected brain cells confers only one part of the brain's processing power, for along with nerve cells there are over five times as many smaller **glia** cells. All these cells have numerous fine branches extending from them to form interconnections with other nerve cells: some individual cells may have several hundred connections, others several thousand and in the cerebellum certain cells may have one hundred thousand connections. The number of interconnections has been estimated to be of the order of 50 trillion (50×10^{15}). Nor is this the whole story. Memory storage in the brain seems to involve changes in the protein molecules associated with the nerve cells. Additionally, certain glia cells are not fixed relative to adjacent brain cells but may move into active areas of the brain, thus modifying the brain's structure in response to incoming stimuli. Glia cells, unlike larger brain cells, have the ability to subdivide as well as move, so that their number and distribution may change depending upon the activities of the brain.

What makes the human brain so interesting is that the owner is, to some extent, able to observe his/her mental states and decide upon a course of action thereby. This course of action is not unchangeable but open to modification. Even though humans have characteristic patterns of behaviour by which they may be recognized as individuals, it is still possible for a person to examine past behaviours and bring about a change for no other reason than that a change is regarded as desirable. This capacity makes human behaviour notoriously unpredictable even when we know a person very well. This is not the same as Turing's[3] suggested incorporation into a machine of a 'random element' consisting of a random number series which produces changes in the behaviour of the machine. In human terms, such a random element would be more characteristic of psychotic human behaviour, where there may be an absence of awareness of the behaviour on the part of the psychotic and little appreciation of its effect upon others. Self awareness is the ability that gives humans the capacity for controlled variability and includes intentionality and appreciation of causality.

The origin of self awareness

Although it is difficult to be specific on this point since we no longer remember what we experienced in the few months preceding our birth, it is possible to conjecture that our sense of 'self' begins to develop quite some time before birth. Acoustic images of developing foetuses show them yawning, moving, sucking their thumbs, etc., indicating the presence of kinaesthetic and tactile awareness. There seems little doubt that, like Tristram Shandy, we are responding to, and becoming aware of, our own bodies in relation to the environment surrounding us. In other words, we are developing self awareness.

Self awareness includes the development of body image, that is, the knowledge that our bodies are unique, yielding sensations that are related to each other. Visual and tactile investigation by a young baby of its body yields a complex integrated pattern of sensations that, in conjunction with kinaesthetic feedback from muscles and joints, gives the child a sense of personal identity that is different from all other objects in the environment: other objects are regarded as external to the self. To achieve this development of body image, the child must **move** relative to the environment, so that it experiences variations in the size of objects as distance changes and variations in shape as viewing angles change. Both the distance information gathering senses of vision and hearing are co-ordinated with the body senses of touch, pressure, pain, temperature and kinaesthetic feedback, to produce an organized pattern of information resulting in

self awareness.

The experiment by Held and Hein (1963)[4] with kittens indicates that visual ability requires integration of changing visual patterns (brought about by moving in the environment) with simultaneous stimulation of body senses and locomotor activity on the part of the animal. In this experiment, two kittens were kept in the dark until their eyes opened. Then they were placed at opposite ends of a bar pivoted at its centre so that it could rotate. Only one kitten, 'A', had its feet on the floor and so could walk around in a circle. It could also turn around on the spot because of the design of the apparatus. The other kitten, 'B', stood in a basket that prevented foot contact with the floor but, because of an interlinking system of gears and chains, it was moved whenever kitten A moved: it could not initiate movement itself. Both kittens therefore received similar visual stimulation. When the kittens were released after 30 hours, kitten A could make normal visual responses, such as avoiding a cliff, blinking to avoid an object approaching the eye and avoid obstacles. Kitten B was unable to do any of these tasks and only learned to see when allowed to walk.

It has been stated that "artifical intelligence is the study of computer programs" (Boden)[5]. In humans, it would perhaps be more accurate to say that intelligence is a function of the **body** and equates with sensitvity to external and internal stimuli. The new born baby has no program derived from outside sources, although it shows responses: exhibiting sensitivity to (and reflex movements away from) painful stimuli. Light and sound convey little meaning at this stage; learning is initially related to the body senses. For example, if the baby makes random movements of the hands, it may strike the side of the cot and receive a sensation in that hand. If the baby strikes its own face, it receives a sensation in the face as well as in the hand. This is a unique experience different from all other contacts with the world outside the individual's body. The baby soon associates these sensory inputs with the internally derived sensations from the muscles that are involved in making the movements, so from the beginning sensory information establishes a complex body image. This is later extended to include visual and auditory patterns and rapid learning occurs. It is worth noting that language need not be involved. A deaf child exhibits intelligent behaviour solely by observation of the environment: recognition of a person's facial expressions or gestures is an early form of communication. In humans, simple signals and signs later become more complex to include written and verbal symbolization so developing into language as used in the conventional sense. It is at this level of symbolization that it becomes possible to manipulate words or numbers as models of the environment. The usefulness of the scientific method has depended upon establishing an accurate correspondence between symbols and reality. When the symbols no longer do the job of predicting or explaining, one returns to the experiment as exemplified by Faraday[6].

There is a danger that the symbols may be regarded as the repository of intelligence, when in fact the symbols only exist because of the intelligence used to construct them initially. Mechanical manipulation of symbols according to the rules of language may bring benefits in solving problems, but the program responsible for the manipulation (itself a language) lacks the attributes of self awareness and sensitivity to the environment that characterize human intelligence.

Brain and machine translations

A machine may reproduce functions that may be similar to human ones, for instance, translating English into French. The process of translation is established by comparison of the two sets of visual symbols, since the languages follow very similar patterns. Languages describe the variables in our environment and these are, in most physical aspects, common to all societies. The same things are given different symbols (either auditory in the case of speech or visual in the case of written language). The dynamics of events in the environment are also constant: 'a girl runs', 'an object falls', 'a goat jumps', and so on. Therefore, translation involves matching two symbolic patterns, but to produce language, a perceptive organism must first observe the environment and establish a linguistic model of the 'real world', which may be used for interchange of ideas. In the case of a second language, some important similarities are established, for instance, finding what symbols in French stand for man, woman, girl, goat, etc., after which translation is relatively easy because of the communality of experience of the environment embodied in human languages. The translation of Egyptian hieroglyphics was not possible until the discovery of the Rosetta stone where the same message had been recorded in hieroglyphics, Greek and Coptic. The recognition of the name of Ptolemy, which occurred in all these versions, made it possible for Champollion to equate the unknown hieroglyphics with a known language and so produce a translation. Languages have contained within them a causal pattern echoing the environment from which the language was derived.

The interesting aspect of languages is that once they have been established, they may be processed in a variety of different ways because of the built-in degree of correspondence to our world, which makes them useful tools. However, language can not express unambiguously all aspects of the real world since linguistic concepts of language (including mathematics) relate to generalities and not specifics. Linguistic devices may be used to define a particular dog as spaniel, but specificity requires more descriptive information. We soon reach a point where language is no longer capable of conveying the information that a few seconds' direct contact with the dog would provide. State of health, condition of coat, friendly or not, does it like you, how old is it, how heavy, etc. Language is a substitute for reality, and this limitation extends to all descriptive applications.

The problem of ascribing intelligence to a device that solely processes language is revealed if a nonsense-language is used. The machine may produce 'solutions' to nonsense problems fed into it (following a set of rules), but these would be meaningless. The machine is no less capable than machines using real language, nor is its program less complex. The only difference between a nonsense machine and a language processing machine is the degree of correspondence of the symbols used to our environment and this is something that an external observer perceives. This is intelligence by implication, that is, the recognition that certain activities resemble (or differ from) human intelligence: in the case of language processing, intelligence is a function of neither the machine nor the program.

If a black box processes problems, it is tempting to regard the machine (or program) as intelligent since its behaviour resembles that of intelligent humans. If the black box is enlarged to make a room capable of housing hundreds of thousands of people, these may be arranged to process information in the same way as a machine. Chains of individuals handle the input, make available stored information and present an output as a machine does. In this case, where does the intelligence lie? The grouping of individuals is analogous to the circuitry of a machine, but no 'group intelligence' is generated simply by the use of a number of individuals. The instructions to the subjects are carried out by the occupants of the room, but each person is simply carrying out part-functions, the implications of which are not recognizable since their relation to other functions is not apparent. The program

represents the instructions that the workers are carrying out. Intelligent performance is recognizable only by observing the performance of the whole group. Intelligence then is not in the program itself, but in the way the program was designed. This suggests that it is possible to design a machine that performs according to its programming in an apparently intelligent way without it necessarily being intelligent. The machine would need to organize its behaviour by itself, monitor the environment and be responsive to it and be aware that it was doing so if its behaviour were to be equated with human intelligence.

Intelligence

A definition used by Alfred Binet involves at least four factors:

1. **Direction** – the ability to set up a goal and work toward it;
2. **Adaptability** – the ability to adapt onself to the problem and use appropriate means to solve it;
3. **Comprehension** – the ability to understand the problem;
4. **Self evaluation** – the ability to evaluate one's performance and to determine the correctness of approach.

Examples of intelligence in humans cover an enormous number of activities ranging from simple identification of objects to solving complex problems involving the practical manipulation of equipment and the development of theoretical models (based on the result of experimentation). This involves both language and mathematics.

In Binet's factor of self-evaluation, the concept of self awareness is implicit since to evaluate one's own performance requires that one must be aware of what the performance was, who the performer was and that the evaluator of the performance was the original performer. This type of self-analysis with its recognition of individual identity is a fundamental feature of human intelligent behaviour. Occasionally one finds in the literature reference to 'idiots savants'. Really, the term is self-contradictory since idiocy and sagacity are mutually incompatible. The term is used to describe those individuals who, while showing limited general intelligence, are somehow able to perform brilliantly in a specific area, for example, adding up large columns of figures, or working out the day on which a particular date falls in the calendar fifty years hence, etc. In human terms, they would not be regarded as intelligent but rather as having a processing facility for certain data. Wechsler[7] described intelligence as the purposeful and rational ability to deal with the environment. Human intelligence requires that an individual be able to interact with the environment, perceive relationships, predict events and be aware of the effect of his/her actions on others. This is an example of primary intelligence. Symbolic representations in the form of language and mathematics are evolved later as convenient tools for processing information derived from primary intelligence. As stated earlier, when symbolic systems have been constructed, these lend themselves to processing in a variety of different ways, but they are the outcome of intelligence rather than intelligence per se. Terms such as cognitive science or artifical intelligence as applied to the processing of symbols refer to aspects of human abilities and there is a danger in attributing too much to processing functions solely on the grounds that they reflect some aspects of human intelligence.

In the introduction to his book on intentionality, Searle has argued for the inclusion of mental activities when concepts such as intentionality are considered; he rejects "any form of behaviourism or functionalism, including Turing machine funactionalism, that ends up by denying the specifically mental properties of mental phenomena". My own thoughts from a psychological viewpoint also stress caution in reading too much into machine performance, since there is a danger of establishing a form of anthropomorphism that may militate against exploration of human brain functions by model making.

Systems of linguistic analysis and response are closed systems (at present). Once the rules are provided, behaviour is determined by the logic of the system, even though changes in patterns may be affected by the introduction of new data. Self awareness would represent a constant monitoring by the system of its performance in relation to the world outside and to itself. Some aspects of social self awareness are outlined by Duval and Wicklund (1972), Argyle (1969) and Fenigstein, Scheier and Buss (1975)[8].

Elements introduced by human self awareness are not necessarily logical or related to a predetermined goal of efficiency or accuracy. Departures from a logical path may be brought about by the recognition of similarity between the 'individual' and other individuals (which is the beginning of social intelligence and moral responsibility). Emotions such as pity, compassion, love, etc., may produce departures from a logical behaviour pattern since self awareness links all forms of behaviours with oneself. Ethical considerations involving feelings of empathy for others arise, involving both animals and humans. 'If I were a gorilla, would I like my habitat destroyed?', and so on. Introspection brings a new level of internal control of behaviours that may seem unintelligent (when in love, for instance), yet each behaviour is intelligent within the framework of the individual's perception of his/her feelings. The list of human attributes that may influence intelligent behaviour is enormous and includes, along with love, altruism, self-sacrifice, admiration, aesthetic appreciation, and so on. Without such sensitivity to environmental factors, it would be difficult to argue that intelligence was at work. The current conflict between developers and conservationists is an outcome of a wider intelligence coming into conflict with commercial intelligence. It would seem prudent from the outset that exploration into the areas of cognitive science and artificial intelligence should not be restricted to a narrow spectrum, but should attempt to deal with the wider issues involved in intelligent behaviour.

References

1. "Artifical Intelligence", M. Seymour, *Elektor Electronics*, May 1988, pp. 38–40.

2. *Intentionality: an Essay in the Philosophy of Mind*, John R. Searle, CUP 1983.

3. *Alan M. Turing*, p. 133, Sara Turing, W. Heffer & Sons, 1959.

4. "Movement produced stimulation in the development of visually guided behaviour" R. Held and A. Hein, *Journal of Comparative and Physiological Psychology*, 56. 872–876, 1963.

5. *Artifical Intelligence and Natural Man*, p. 3, Margaret Boden, The Harvester Press, Hassocks.

6. *Michael Faraday: a Biography*, L. Pearce Williams, Chapman and Hall, 1965.

7. *The Measurement and Appraisal of Adult Intelligence*, D. Wechsler, Williams and Wilkins (1958), Baltimore Md.

"Intelligence defined and undefined: a relativistic appraisal", D. Wechsler, *American Psychol.*, 30, 135–139 (1975).

8. "Public and Private Self Consciousness: Assessment and Theory", A. Fenigstein, M.F. Scheier and A.H. Buss, *Journal of Consulting and Clinical Psychology*, 43, 4, 522–527 (1975)..

Social Interaction, M. Argyle, Atherton Press (1969), New York.

A Theory of Objective Self Awareness, S. Duval and R.A. Wicklund, Academic Press (1972) New YHork.

DC-DC POWER CONVERTER

T. Wigmore

This high-efficiency step-up converter supplies up to 30 V at 75 W when powered from a 12 V car battery. The converter is ideal for many mobile and other out-of-doors applications: it functions as a power source for your DC-operated soldering iron, RF power amplifier, or NiCd battery charger for portable equipment such as a flasher or a video camera.

DC-DC converters for stepping up the car battery voltage are generally based on a switched-mode power supply (SMPSU) or a power multivibrator driving a transformer. The power converter described here is based on the first principle, and uses the Type TL497A integrated circuit from Texas Instruments. This device enables good voltage regulation with low output noise to be achieved fairly easily, and in addition guarantees a relatively high conversion efficiency.

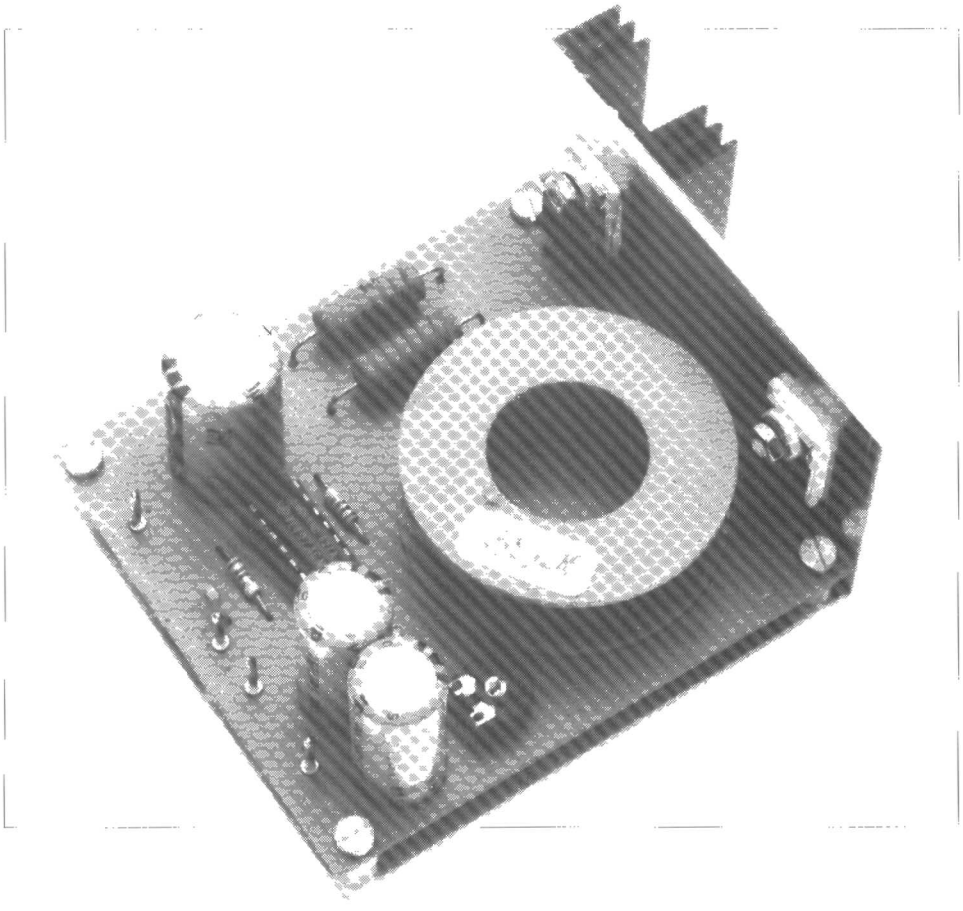
- Flyback-type step-up converter
- no special inductor required
- input voltage: 12 VDC
- output voltage adjustable between 20 and 30 V
- maximum output power: 75 W
- efficiency: 70%, independent of load current
- voltage reduction at load variation from zero to maximum: <200 mV
- ripple voltage: <500 mV_{pp}.

Design background

The converter described is of the flyback type. The flyback principle is the only practical way of generating a direct output voltage from a lower direct input voltage.

The central switching element in the converter is power SIPMOS transistor T_1 (see Fig. 1). When it conducts, the current through L_1 rises linearly with time. During the on-time, magnetic energy is stored in the inductor. The moment the transistor is turned off, the inductor functions as a source of magnetic energy, which is supplied as an electric current to the load via D_1. In this process, it is important that the transistor remains off during the time taken by the magnetic field to decay to zero. When this condition is not met, the current through the inductor rises to the saturation level. An avalanche effect then causes the current to increase very rapidly. The relative on-time, or duty factor, of the transistor control signal must, therefore, not be allowed to reach the value of one.

The highest permissible duty factor is dependent, among other factors, on the output voltage, because this determines the rate of decay of the magnetic field strength. The maximum output power that can be supplied by the converter is governed by the maximum permissible peak current through the inductor, and the frequency of the switching signal. The limiting factors here are mainly the saturation instant and the maximum tolerable ratings for the copper losses in the inductor, and the peak current through the switching transistor (remember that a 'burst' of a particular energy content is supplied to the output at each switching period).



TL497A

The operation of this integrated circuit is rather unconventional, so that a brief description is given below.

In contrast to widely used *fixed frequency, variable duty-factor* SMPSU controller ICs, the TL497A is qualified as a *fixed on-time, variable frequency* device. This means that the duty factor is controlled by means of frequency variation to maintain a constant output voltage. This method results in a fairly simple circuit, but has the disadvantage of the switching frequency reaching down into the audible range when the load current is low. In actual fact, the switching frequency becomes lower than 1 Hz when the converter is not loaded. The slow ticks heard as a result are the charge pulses applied to the output capacitors to maintain a constant output voltage. In the absence of a load, the output capacitors are, of course, slowly discharged by the voltage sensing resistors.

The on-time of the oscillator on board the TL497A is fixed, and determined by C_1. The oscillator may be disabled in three ways: first, if the voltage at pin 1 exceeds the reference voltage (1.2 V); second, if the current through the inductor exceeds a certain maximum; and third, via the in-

hibit input (this is not used here).

During normal operation, the oscillator causes T_1 to conduct so that the inductor current rises linearly. When T_1 is switched off, the magnetic energy stored in the inductor is used to charge the output capacitors. The output voltage, and with it the voltage at pin 1 of the TL497A, rises a little, so that the oscillator is disabled until the output voltage has dropped to a sufficiently low level. This process is repeated cyclically, at least, in theory.

In a configuration with real components, however, the voltage rise caused by the charging of the capacitors within one oscillator period is so small that the oscillator remains enabled until the inductor current reaches the maximum value defined with R_2 and R_3 (the voltage drop across R_2 and R_3 is 0.7 V at this stage). The current rises in steps as shown in Fig. 2b because the duty factor of the oscillator signal is greater than 0.5.

When the maximum current is reached, the oscillator is disabled, and the inductor is allowed to pass its energy to the capacitors. In this condition, the output voltage rises to a level high enough to keep the oscillator disabled via pin 1. The output voltage drops, and a new charge cycle commences.

Unfortunately, the switching operations outlined above are coupled to relatively high losses. In a practical application, this problem is resolved by making the on-time (i.e., C_1) large enough to ensure that the inductor current does reach the maximum within a single oscillator period (see Fig. 3). The solution in this case is the use of an air-cored inductor, which has a relatively low self-inductance.

Some waveforms

The timing diagrams in Fig. 3 show the signal waveforms at the main points in the circuit. The central oscillator in the TL497A operates at a low frequency (lower than 1 Hz if the converter is not loaded). The switch-on instant, shown as the rectangular pulse in Fig. 3a, is determined by capacitor C_1. The switch-off time is determined by the load current. During the on-time, T_1 conducts so that the inductor current rises (Fig. 3b). In the non-conductive period after the current pulse, the inductor functions as a current source. The TL497A compares the attenuated output voltage at pin 1 with its internal reference voltage of 1.2 V. If the measured voltage is smaller than the reference voltage, T_1 is driven hard again to enable the inductor to store energy.

The above charge and discharge cycles cause some ripple voltage on the output capacitors (Fig. 3c). The feedback arrangement enables the oscillator frequency to be adjusted for optimum compensation of voltage losses caused by the load current.

The timing diagram in Fig. 3d shows considerable swing of the drain voltage owing to the relatively high Q (quality) factor of the inductor. Although the parasitic oscillations do not affect the normal operation of the power converter, they may be damped with the aid of a 1 kΩ resistor in parallel with the inductor.

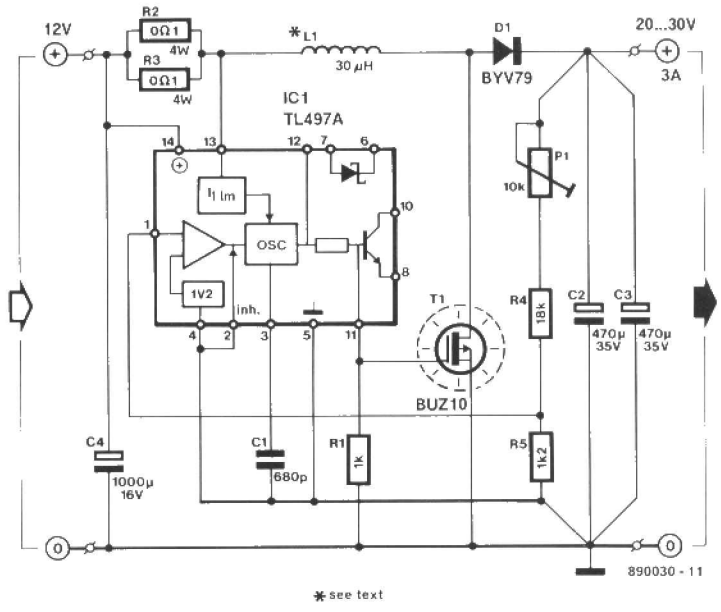


Fig. 1. Circuit diagram of the step-up converter.

From theory to practice

Naturally, a switch-mode power supply is designed for maximum rather than quiescent output current. High efficiency and a stable output voltage with little ripple are also prime design goals.

In general, the load regulation characteristics of a flyback type switch-mode power supply give little cause for concern. During every cycle, the on/off ratio is adjusted in accordance with the load current, so that the output voltage remains fairly stable in spite of large load current variations.

The situation looks a little different as far as the overall efficiency is concerned. A step-up converter of the flyback type typically generates relatively large current surges, which cause considerable power losses (remember that power rises exponentially with current). In practice, however, the proposed converter has a total efficiency higher than 70% at maximum output current, which is remarkable given the simplicity of the design.

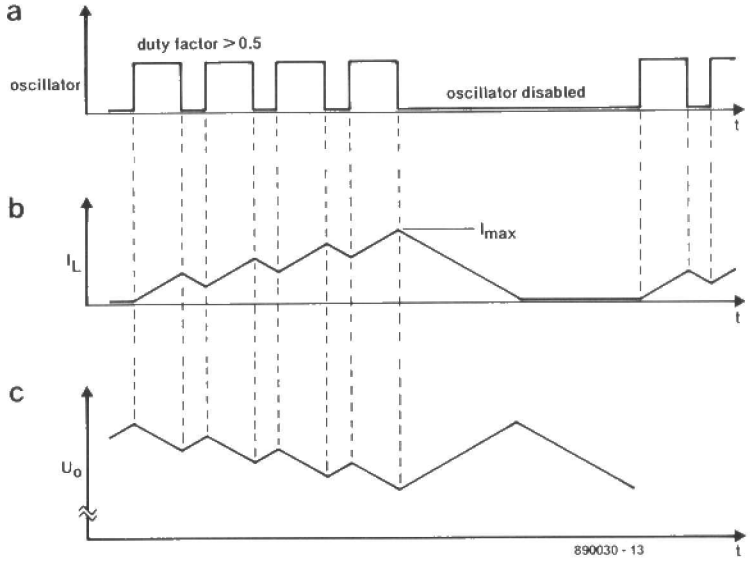


Fig. 2. Showing how the inductor energy is built up under the control of the oscillator signal.

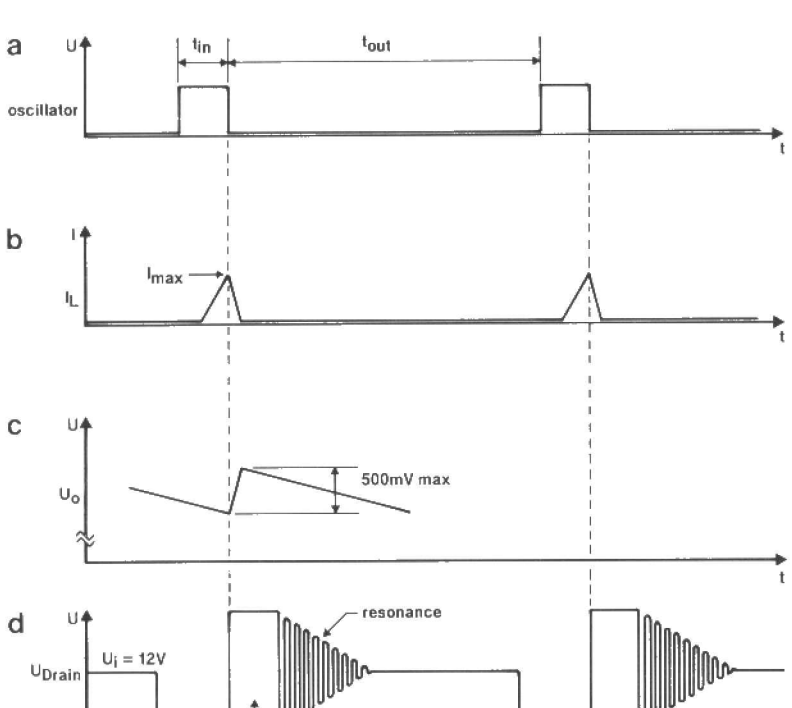


Fig. 3. Timing diagrams of the main signals in the circuit. The current reaches its maximum value within one period of the oscillator signal.

The switching frequency at maximum load is made as high as possible to allow the use of a relatively small self-inductance. The practical circuit is based on an air-cored inductor. Significant losses caused by a ferrite core are thus avoided.

A fast power-FET of the SIPMOS type is used to switch the inductor current. The Type BUZ10 or BUZ10A was chosen because of its short recovery time. To achieve acceptable efficiency, the transistor must be used as a switching element.

Parts list

Resistors (±5%):
R_1 = 1k0
R_2;R_3 = 0Ω1; 4 W
R_4 = 18kΩ
R_5 = 1k2
P_1 = 10kΩ preset H

Capacitors:
C_1 = 680p
C_2;C_3 = 470µ; 35 V; radial
C_4 = 1000µ; 16 V; radial

Inductor:
L_1 = 30 µH (home-made, see text)

Semiconductors:
D_1 = BYV79
T_1= BUZ10 or BUZ10A
IC_1 = TL497A

Miscellaneous:
Heat-sink for T_1.
PCB Type 890030 (not available through the Readers Services).

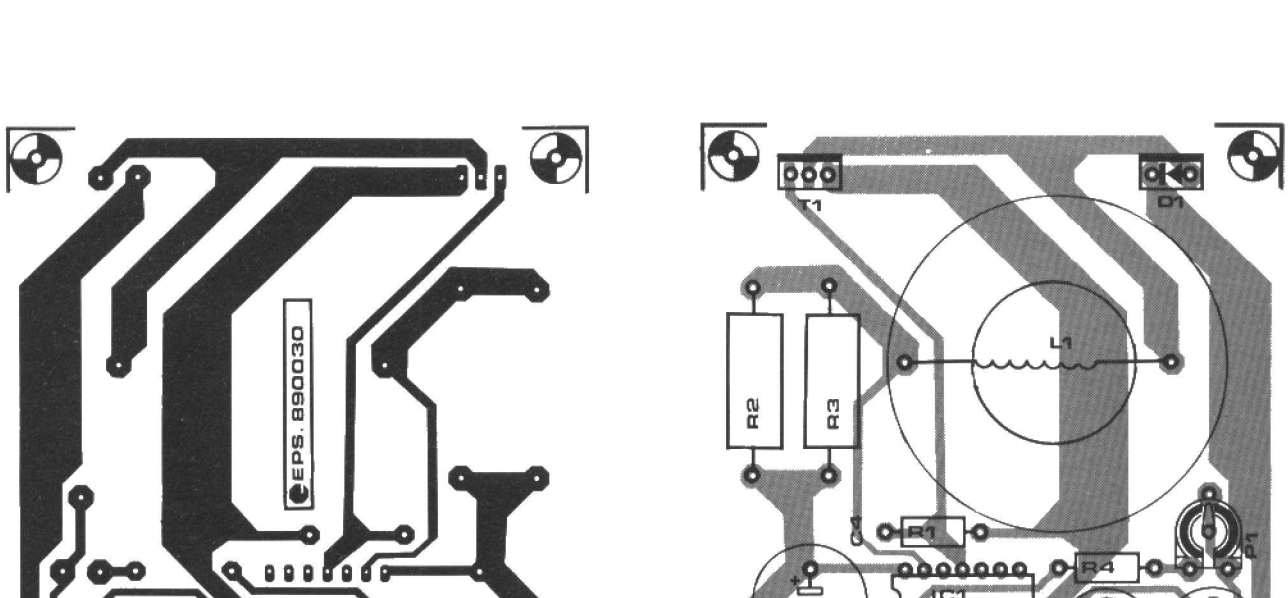


Fig. 4. Printed-circuit board for the DC–DC converter.

This, in turn, requires it to be driven into saturation, resulting in a relatively long turn-off time. Obviously, the longer it takes for the transistor to interrupt the inductor current, the lower the overall efficiency of the converter. Unconventionally, the BUZ10 is driven by the oscillator test-output of the TL497A (pin 11) rather than the internal output transistor.

Diode D_1 is another essential part in the circuit. The requirements for this device are an ability to withstand high current surges, and a low forward drop. The Type BYV79 meets these conditions, and must not be replaced with a general-purpose type.

Returning to the circuit diagram of Fig. 1, it should be borne in mind that current peaks of 15–20 A are not uncommon in the circuit. To prevent problems arising with batteries having a relatively high internal resistance, capacitor C_4 forms a buffer at the input of the converter. Since the converter charges the output capacitors with short, surge-like current pulses, two capacitors are connected in parallel to ensure that stray capacitance remains as low as possible.

The power converter is *not* short-circuit resistant. Short-circuiting the output terminals is the same as short-circuiting the battery via D_1 and L_1. The self-inductance of L_1 is not so high as to limit the current for the time required by a fuse to blow.

A home-made inductor

Inductor L_1 is wound from 33½ turns of enamelled copper wire. Figure 5 shows the dimensions. Most manufacturers supply enamelled copper wire on an ABS reel,

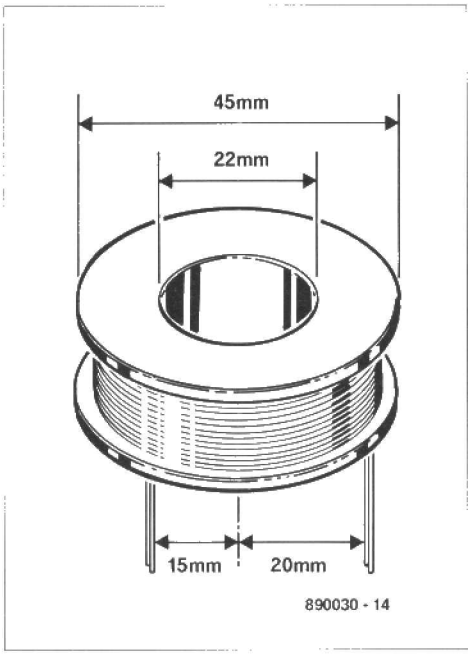


Fig. 5. Suggested construction of the inductor on an ABS reel.

which is suitable as the former for making the inductor. Drill two 2 mm holes in the lower rim to pass the inductor wires: one hole beside the cylinder and the other at the outside of the rim.

There is little point in using thick wire to wind the inductor, because the skin-effect, i.e., the displacement of charge carriers towards the outside of the wire, must be taken into account given the frequencies used in the converter. To ensure a low resistance at the required inductance, it is recommended to use two wires of 1 mm diameter, or even three or four wires of 0.8 mm diameter in parallel. Three 0.8 mm wires result in a total diameter that is roughly the same as that of two 1 mm wires, but has the advantage of resulting in a 20% larger effective surface.

The inductor is close-wound and may be encapsulated in a suitable resin or potting compound to limit the sound level (remember that the frequency of operation is within the audible range).

Construction and alignment

The printed-circuit board designed for the DC-DC converter is shown in Fig. 4. A number of constructional points require attention.

Resistors R_2 and R_3 run fairly hot and must, therefore, be mounted at a few millimeters above the board surface. The peak current through these resistors can be as high as 15 A. The power-FET also runs hot, and requires a medium-size heat-sink and the usual insulating material. The diode can do without cooling, although it is conveniently bolted on to the same heat-sink as the power-FET (do not forget to insulate it electrically). During normal operation, the inductor heats up.

Heavy-duty terminals and wires must be used at the input and output of the converter. The battery is protected by a 16 A delayed action fuse inserted in the input supply line. Remember that the fuse does not protect the converter!

The circuit is simple to align: adjust P_1 for the desired output voltage between 20 and 30 V. The output voltage may be made lower, but not lower than the input voltage, by using a smaller resistor in position R_4. The maximum output current is about 3 A.

CORRECTION

"Simple Transmission Line Experiments"

(September 1989, p. 38)

Some serious errors have crept into the translation of the author's sketches into the published illustrations. Unfortunately, since the final proofs sent to author were apparently lost in the mail, these errors remained undetected until the magazine was printed. It should, therefore, be clear that the errors can not be attributed to the author.

Corrected illustrations are shown here, but for clarity's sake the errors in the originally published article are:

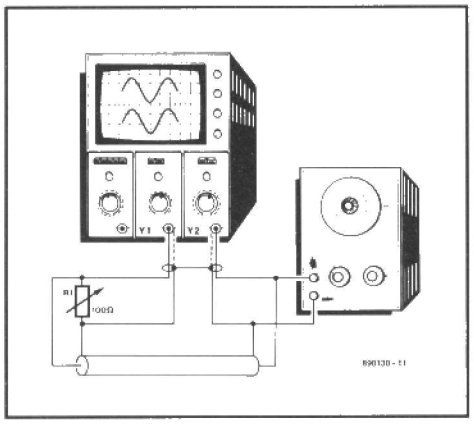


Fig. 1.

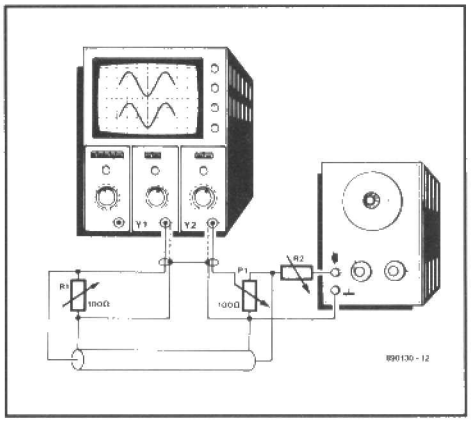


Fig. 2.

1. the Lissajous' figures shown on the oscilloscope give a false impression: they are NOT used;

2. it is not clear that the Y-amplifiers on the oscilloscopes have coaxial inputs: the first impression may well be that two wires are connected to a single input;

3. the connections to the signal generators give the false impression that the earth line is connected to the upper terminal, whereas, where such instruments have 4 mm terminals, one above the other, it is always the lower one that is at earth potential.

We apologize to the author and those readers who may have been inconvenienced by these errors.

PERSONAL COMPUTER DECISIONS

by Linda Bishop*

In choosing a PC system, the key question is not so much which processor platform is the 'best', but rather which is the most appropriate platform for you. It is not simply a choice of speed either. Memory access and multitasking capability must also be considered in a platform decision. And then, of course, there's software. What type of applications will you run? What operating system do you need? In software, as in the platform decision, several criteria should be explored: price, performance, applications and the future. OS / 2 addresses all these issues.

OS / 2 allows multi-tasking, multi-user operation, breaks the 640 K barrier of DOS and supports the graphical user interface of presentation manager. This will make network communication easier, provide bigger databases, more complete and simple applications, and allow computers to do several things at the same time.

What makes OS / 2 unique is that it is the first full-fledged multi-tasking system for the 80286 microprocessor that can switch back and forth between protected mode and real mode to run the new programs designed for OS / 2 as well as most existing DOS programs.This will give DOS users a smooth upgrade path to OS / 2.

The built-in network support of OS / 2 allows multi-user operation: this facility of having several programs running at the same time is, of course, a most useful one. Moreover, OS / 2 permits distributed applications, that is, it allows the program in your PC to work (communicate) with programs in other PCs.

OS / 2 was written for the 80286 processor, taking advantage of the special protected mode feature. This feature is also provided by the 80386. OS / 2 was not written to take advantage of any of the new features of the 80386 and no performance advantages are obtained by running OS / 2 applications on an 80386.

The 80386 is no faster than an 80286 when running 16-bit software at the same clock speed. The primary reason for this is that the 80286 executes more 16-bit instructions in fewer clock cycles than the 80386 or 80386SX. Out of 190 existing 16-bit instructions, the 80286 is faster on 74, the 80386 is faster on 50 and the two devices are the same on 66 instructions. In fact, the only way the 80386 is able to run OS / 2 at all is by emulating the 80286.

The applications that are available today as well as those currently being developed will not take advantage of the 80386 until an OS / 386 specific version of the operating system is available some time next year: OS / 386 general applications are planned to become available sometime in 1991-92.

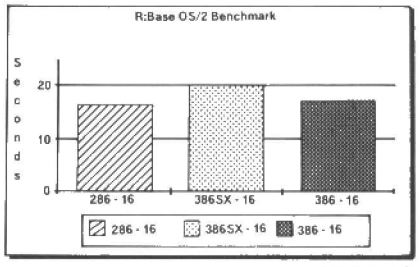
Once an 32-bit operating system is available for the 80386, the device will have an advantage over the 80286. But there is no guarantee that 80386, and especially 80386SX, personal computers available now have the configuration to run new 80386 32-bit software four years from now. After all, the first 80286-based PC sold several years ago at 6 MHz with 640 K of memory is hardly suitable for running 16-bit OS / 2 now. The same situation is likely to exist in four years' time for today's 80386 PC as far as running 32-bit 80386SX software is concerned.

What is important for the OS / 2 operating system then is not whether it is run on an 80286 or an 80386, but rather the speed of the processor. The bulk of the processor's work is multi-tasking, that is, the accomplishing of several things at the same time by dividing the computer's time into 'time slices' that last only a fraction of a second. These time slices are handled so fast that it appears as if programs are run simultaneously. Since the processor is actually carrying out all the tasks at separate intervals (time slices), the faster the processor, the quicker the multiple tasks will be completed. An adequately equipped 80286 system running at least 12–16 MHz with VGA (Video Graphics Array) graphics forms a very cost effective OS / 2 foundation .

* Linda Bishop is a product marketing engineer for Advanced Micro Devices' Personal Computer Products Division, Austin, Texas. She received her BSEE from the University of Michigan (Dearborn). Prior to joining AMD, she worked for Motorola.

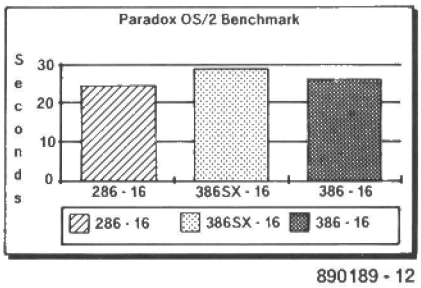
High-speed system pricing
80286 vs 80386

	286-20	386-20	Difference
Dell	$2,999	$4,099	37%
Zeos	$2,095	$2,995	43%
Northgate	$2,599	$3,699	42%
PC Brand	$2,379	$2,995	26%
Dataworld	$1,555	$1,995	28%
CompuAdd	$1,695	$2,295	35%



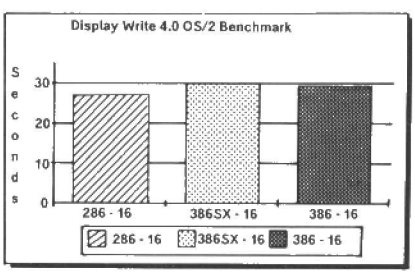
890189 - 11

Figure 1



890189 - 12

Figure 2



890189 - 13

Figure 3

The 80286 system offers everything for the needs of today's and tomorrow's user. Fast 80286 (16, 20 and 25 MHz) systems available now have the 16 Mbyte memory access capability and the protect mode for multiple applications required of OS / 2.

The 80286 is one of the best-selling processors on the market today and it is widely available. Moreover, its price is at an economical level for the system designer.

Owing to its die size, packaging and complex processing, the 80386 is more expensive. Moreover, systems built around this device require 32-bit peripherals: the design cost is, therefore, higher as well.

This leads to significant price differences between identically configured 80286-based and 80386-based personal computers. As shown in the table, an 80386-based system costs on average 35% more than an 80286-based system.

The 80286 and 80386SX PCs used in the tests to arrive at the comparison bar graphs in Fig. 1, 2 and 3 are Everex STEP models, while the 80386 is an IBM System 80. The 80386 PC uses page mode memory access for 0.8 average wait states with 80 ns DRAMS. Both the 80286 and the 80386SX run zero wait state with 60 ns DRAMS. The performance of these PCs is indicative of that of other PCs.

The benchmark in Fig. 1 is based on the R:Base database program. The source database used is PC Magazine's Index for Volume 4.0. First, a Grouping Select Query (SQL) was performed, followed by a category tally to count the number of occurrences in a category. Next, a calculation loop was performed on the first 100 records. The results are shown in seconds. The bar graphs show that the 80286 PC outperformed the 80386 PC by 4%, while the 80386SX was 24% slower.

The bar graphs in Fig. 2 are obtained from running the Paradox database program on the three computers. The source database is again PC Magazine's Index Volume 4.0. First, a Grouping Select Query was performed. Next, a report was run with the output sent to a file on RAM disk. The query results were then sorted and a conditional delete of the records in the query results was performed. The results are shown in seconds. As is seen, the 80286 PC was 18% faster than the 80386SX.

The comparative tests illustrated in Fig. 3 were based on the IBM word processor program Display Write 4.2. The benchmark started with a 100 K, 40-page document. A global search and replace was performed, changing one frequently used word for another. Next, the margins were narrowed, forcing a complete text rewrap. Lastly, the document was repaginated. The results are shown in seconds. Again, the 80286 PC was faster than the 80386 PC by 4%, while the 80386SX was 8% slower than the 80286 PC.

Comparative tests are influenced both by the processor and by the memory interface. In the PC systems used, the memory interfaces were relatively equal (0.8 wait states on the 80386 and 0 wait state on the 80286 and 80386SX machines). Thus, the performance difference measured between the 80286 and 80386SX was caused solely by the different processors with the former performing faster than the latter.

The performance difference between the 80286 and 80386 must take into account the different memory interface techniques. A 0.8 wait state system (as on the 80386 PC) has about a 9% performance degradation compared to a true zero wait state system (as on the 80286 PC). Taking this into account, the 80286 and 80386 systems performed essentially the same.

As OS / 2 software becomes more prevalent, PC performance will become more important. Performance is primarily a function of processor clock speed and memory interface in the PC. Clock speeds of 16 MHz and beyond will be needed to run multiple applications effectively. It should be borne in mind that there is little difference in performance between the 80286 and 80386 running at the same clock speed on OS / 2.

In addition to performance, price will also remain a major factor in personal computer decisions and it was seen that 80286-based PCs remain substantially cheaper than 80386-based systems. The 80286 has, moreover, a lot of life left for DOS, as well as OS / 2, systems and will continue the trend toward higher clock speeds.

According to Dataquest, the 80286 will increase its current market share of IBM and compatible PCs from 30% to 33% by 1992 and become the entry-level PC, replacing 8086/8088 based machines. Following a stable path to OS / 2, the 80286 is the best platform for cost vs performance.

ELECTRONICS SCENE

PICTURE-IN-PICTURE MINIBOARD FROM SIEMENS

The SDA 9088 Picture Insertion Processor from Siemens allows the picture-in-picture facility to be installed not only in digital TV sets, but also in analogue ones. The need for only two chips reduces time and material requirements and increases reliability. The SDA 9088, which is designed in Siemens 1 Mb it DRAM technology, also provides a much better picture quality than previous designs.

The SDA 9088 permits the insertion of a reduced-size picture into the main picture by using picture signals that may be based on completely different standards and synchronization principles. The combination of frame memory, control, digital signal processor and digital-to-analogue converters on a single chip enables equipment manufacturers to realize the picture-in-picture function in TV sets and video recorders on a high-performance and particularly cost-effective basis.

Although the picture-in-picture function has been in existence for some years, it has failed to become widely established in domestic video equipment owing to its high cost, incurred mainly by the expensive but indispensable frame memory and the peripherals required for the analogue-to-digital converters. Through the use of the most up-to-date semiconductor technology, it has now been possible to integrate all essential functions into a single circuit. The primary function of the PIP is to reduce the picture produced by the second picture signal and synchronize it with the main picture.

Two formats are available for the inserted picture: 1/9 and 1/16 the size of the main picture. The insert may be displayed in any of the four corners. A positioner for each corner permits adjustment to the particular set's geometry.

In contrast to previous designs, picture reduction is effected not by omitting the pixels that are not needed but by digital filtering of the horizontal and vertical signals to ensure that all the information is utilized.

The SDA 9088 handles all worldwide TV standards: a detector performs automatic transfer to the standard being received. It is also able to supply standard-converted picture signals at a line frequency of 32 kHz.

SPEEDING UP THE COMPUTER

by Pete Chown

The architecture of the computer

If you look at a modern micro, say, an 80386-based IBM compatible, you will discover that nearly all the memory bandwidth is used up. If faster memory were installed, it might be possible to increase the speed of the processor by several times, but that would be the limit for that particular architecture.

In an earlier article[1] I mentioned one way out of this dilemma: parallel processing. There are, however, many other ways of speeding up apparently sequential processors so that they can reach speeds of up to 600 MFlops (million floating point operations per second). At present, the Cray-3 represents the limit of that approach as far as commercial machines go. The Cray-2 is the fastest one that has been commercially released.

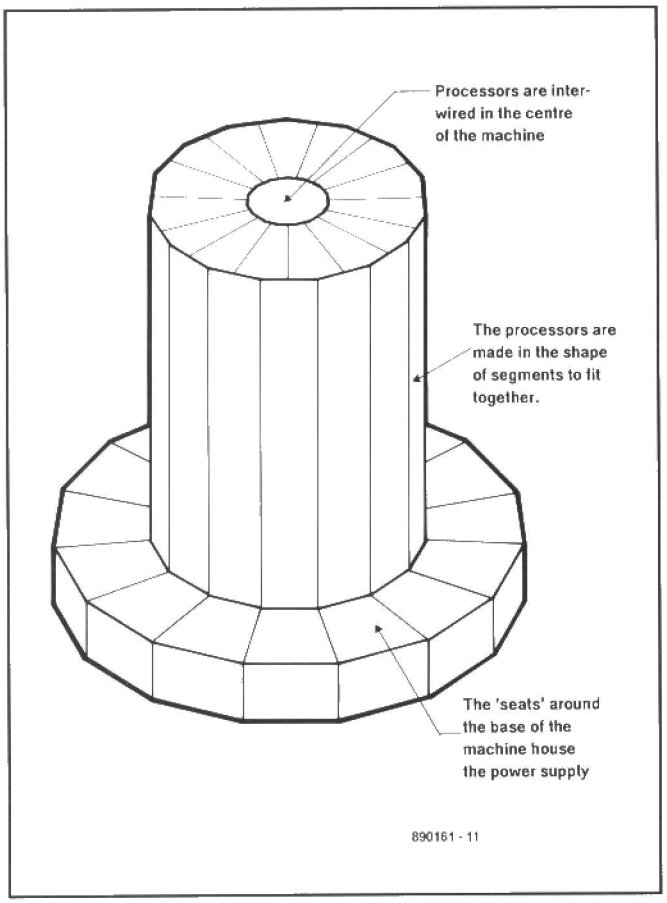
Cacheing

Cacheing is one of the simplest techniques that can be used to speed up a computer. Earlier, I mentioned that faster memory could allow the speed of most machines to be increased substantially. Unfortunately, fast memory costs a disproportionate amount more, and so manufacturers decided to use the fast memory only for instructions that are currently being executed. This means that the cache is loaded with the pages of main memory that are being used (normally in the opposite phase of the processor clock to that on which the processor reads the memory), and it is then available for use.

Using a cache has one other advantage. Memory protection – so that one process can not alter another's memory – is very hard to implement fast enough for the processor's request to access a particular word to be checked in time. On a large machine, only of the order of 100 ns would be available. If a cache is used, however, the system can verify that the process is allowed to use a particular page before it is ever loaded into the cache. A major cause of the inefficient use of caches is that each time the machine switches context (that is, changes the process it is executing) at least part of the cache has to be reloaded.

Multiple processors

Because large machines are generally used for time-sharing, it is quite acceptable for them to incorporate several processors. Generally, however, these share the same bus, so that problems are not encountered with lack of memory on one processor, or problems with an I/O device controlled by another processor. Caches are used to avoid continual conflicts for memory.



Construction of the Cray machines

This tends to be a not very efficient technique, because in practice a large number of conflicts for memory do occur. The best-known machine to use this system is the VAX 8900. It has four processors sharing a bus (each of which is the same as the single processor used in the 8700). Adding a fourth processor does, however, add only about 15% of the performance that the processor would generate on its own. The reason for this is that conflicts for memory mean that the processors are standing idle for much of the time.

The reason that DEC decided to use this technique is probably that it allowed them to keep the same architecture: a radical redesign would have meant changing the instruction set, and the major selling point of the VAX range is that programs for any VAX can be run on any other. The other advantage of this system is right at the top end of the computer market: the US Navy have produced a supercomputer using 16 largely independent processors, giving them the edge over single-processor equivalents.

Pipelining and vector processing

Pipelining and vector processing are other major ways in which manufacturers speed up their computers. They are, however, much more complex to implement than the other systems. The techniques are similar: some computers implement pipelines but not vector processors, but generally speaking the reverse is not true.

In pipelining, the processor, instead of starting on one instruction and executing it to completion, reads instructions continually. Once it has completed reading an instruction, the processor begins fetching the instruction's operands. At the same time, the next instruction will be read, the previous instruction will be executed, and the result of the instruction before that will be written to memory or registers.

In practice, things are not this simple. A pipeline tends to be longer than just indicated, because the aim is to keep the processor-memory interface busy for as much of the time as possible. Since not all instructions need their operands fetched, there would be a tendency for the interface to run out of information to fetch or store.

Problems with pipelines tend to be encountered with jumps. When the processor jumps, everything in the pipeline is useless because it no longer wants to execute those instructions. It is not possible to make the pipeline start taking instructions from the destination of the jump, because the jump might be conditional and the condition would not have been evaluated.

Another problem is when store locations change after the pipeline has been loaded. If one instruction uses the result of

the previous one, the old value that was present at that location in store would already have been loaded. There is no solution to this except the long one – with each and every instruction it must be checked that the operand being loaded is not going to be stored by an instruction already in the pipeline. This is particularly difficult with indirection, because care must be taken that the information about where the operand is coming from is available in time. If it is not, the processor must stop until it is, which leads to inefficiency.

As with caches, pipelines suffer when a processor switches context. Whereas with the cache some of it might be able to be preserved, the entire pipeline must be discarded since there is nowhere for it to be put until the processor returns to that process.

Vector processors take the idea of pipelining a stage further. With large machines providing a large variety of complex mathematical operations, the execution of an instruction is by far the longest step in the pipeline. Consequently, the information about where to find the operands is passed out to a lot of arithmetic processors. This saves the main processor from having to find out what the operands are, or to execute the instruction.

The problems with this are obvious. The difficulties with making sure that the operands of an instruction have not been modified since the instruction was loaded become much worse. Because some instructions complete faster than others, there is a danger of instructions being executed in the wrong order: tens of short instructions could have been executed in the time it takes for a complex floating point function to be evaluated and one of these short instructions might have wanted to use the result of the long one.

Another problem is memory bandwidth – the multiple processor problems are obviously much worse. This has, however, been almost completely solved. Memory, instead of being addressed over a single bus, is addressed on a chip-by-chip basis, so that as long as all the processors wish to access different chips, they can do so at the same time. This solution does, however, lead to another snag: the large amount of wire needed to connect each individual chip!

It is interesting to note that this architecture is based on parallel processing, even though the machines appear sequential to the user. The parallelism is on a very small scale, and so it has been described as 'fine' parallelism, whereas true parallel processing machines have been described as having 'coarse' parallelism.

As these computers get faster, the exact length of wire used to connect two points becomes significant in determining timing. Consequently, Cray Research decided to cut each piece of wire in their machines the same length! Unfortunately, these lengths have to be also as short as possible for the same reason and this led to the circular construction of the Cray machines as illustrated. It also led to the situation where the wires are almost impossible to get at, forming a three-dimensional web of cables that are tight enough for it to be difficult to reach a wire near the middle.

RISC processors

RISC processors are not really viable as a technique for building large machines. The reason is that you are faced with a choice of ways of improving performance – make each instruction do more or execute faster. Small machines had been tending to follow the former route despite the fact that there was not really enough processing power on a single chip to do it. A large increase in speed was therefore obtained when micros began to follow the latter route. Large machines have pipelines, caches and so on, and also aim to do a lot per instruction. Consequently, the Sun, Apollo and Hewlett Packard machines tend to set the limit for this type of technology.

There is now a move to provide a mainframe style processor on a chip, since this is becoming viable with greater reliability and packing density. This will effectively make the RISC processor obsolete in a few years' time, at least as far as the very fastest workstations are concerned.

This trend towards micros that are more like mainframe is actually another way of speeding up computers. We are approaching the limit as far as supercomputers go, but if workstations that only several people use get nearly that fast, they will effectively have a much more powerful machine because there are far fewer processes for it to run.

There will always be a place for the supercomputer, however, in performing single processes that are too complex for a workstation to do. It will, however, become increasingly wasteful to use a supercomputer for a lot of fairly small jobs.

One area of potential for RISC that has not received much attentional is that of arithmetic processing. It would be possible to build a RISC machine with, say, 256 bytes of RAM and several registers that would carry out operations between registers only and not RAM. It would thus be very simple and could, therefore, run at high speeds. It could then be programmed with short, repetitive calculations that could be done over and over again.

Managing a pipeline

I have already discussed some of the problems that arise from pipelining and vector processing. One of the easiest ways to understand the problems and how they are solved is, however, to look at how a vector processor would execute a certain sequence of instructions.

Since this is only for illustration, the instructions will be given in words – not in any form of mnemonic that would make it harder to follow. The instructions are to calculate the coordinates needed to draw a circle by trigonometry. Square brackets indicate indiscretion The label 'pointer' points to a location containing the address where the forty pairs of coordinates are to be placed.

1. Load register A with 0.
2. Load register B with 0.
3. Label:
4. Calculate cos(A), put in register C.
5. Calculate sin(A), put in register D.
6. Multiply C by [radius].
7. Multiply D by [radius].
8. Store register C at [pointer] + B.
9. Store register D at [pointer] + B + 1.
10. Add 2 to B.
11. Add pi/20 to A.
12. Jump to label if A < 2 * pi.

Let us now consider how a vector processor would execute this section of code. It would start by filling its pipeline from the beginning. No evaluation of operands would be necessary for instructions 1 and 2. When these got to be executed, they will be run at the same time because the processor would recognize that they did not refer to the same part of store.

Instructions 4 and 5 could not be executed until instructions 1 and 2 had been completed, because the values of the same registers are used. Once 1 and 2 had been completed, however, they would be executed together.

The same would be true of instructions 6 and 7, but here one of the advantages of a fast processor shows up. The processor has been instructed to look at a particular memory location in order to find the radius of the circle. There is no reason why this should wait to be evaluated until the rest of the instruction can be. Different processors would tackle it in different ways: those with just a pipeline and no vector processor would attempt to find time to evaluate it while the instruction is in the pipeline, while those with a vector processor would simply hand the pointer to one of the arithmetic units and instruct it to look at that place in store.

The two additions would take place concurrently, since they do not refer to each other in any way. The jump would then be encountered. The pipeline would have been unable to follow the jump to its conclusion to get subsequent instructions, because it is a conditional one. It is, therefore, normal for the pipeline controller to

assume that the jump will not be taken, and it will have to abandon all the information it has built up about the instructions following the loop, except when the loop finally ends. Nothing has been lost compared to a conventional processor, however, because the bus would merely have been sitting idle. Once back at the start of the loop it might have kept the instructions because such an eventuality was likely or it might have to start building up its pipeline from scratch again.

Conclusions

Because we are reaching the limits of semiconductor-based computers, the large computer of today is a far more complex thing than its predecessors. The normal rules of structured design have been abandoned in a search for the last megaflop, leading to such peculiarities as computers with all the wires the same length (normally, of course, no one would think of building a large system other than in standard 19 in. rack-mounted cases on a carefully constructed backplane). The techniques do, however, work and we have probably got computers an order of magnitude faster from them. It is, however, a tribute to the people who design them that they work at all.

Human nature being what it is, however, these techniques will probably be with us even when optical computers appear, and we will simply take our thousand times speed increase, and do exactly the same with optical fibres.

References

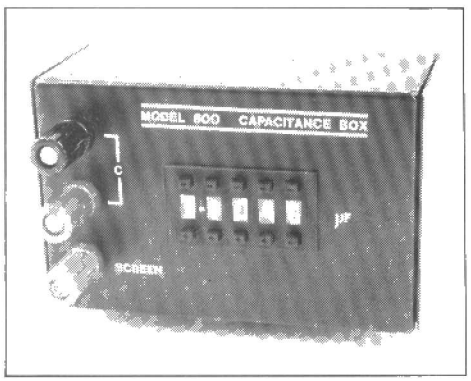
1. "A closer look at the transputer", *Elektor Electronics*, May 1989, p. 39.

NEW PRODUCTS

RESISTANCE BOX AND CAPACITANCE BOX FROM MAPLIN

Maplin have introduced a new resistance box and a new capacitance box, both intended for schools, laboratories and industry.

The Type JL63T six-decade resistance box, priced at £79.95 (incl. VAT), can simulate resistance from 1 Ω to 999,999 Ω in 1 Ω steps very accurately.



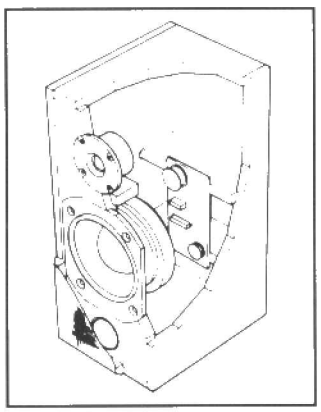
The Type YT55K five-decade capacitance box, priced at £89.95 (incl. VAT), can simulate capacitances from 100 pF to 9.9999 µF in 100 pF steps.

Maplin Electronics • P O Box 3 • RAYLEIGH SS6 8LR • Phone (0702) 554161

VOLT HOME STUDIO MONITOR

Available from Wilmslow Audio is a kit to build the **Volt Home Studio Monitor** loudspeaker. Employing the new VOLT BM220.2 bass unit and the latest Scanspeak tweeter in a compact (33 litre) reflex enclosure, this design has high power handling capability: it will take the full unclipped output of a 200-watt amplifier.

A split-circuit cross-over network enables biwiring to be used without further modification. Eight 30-A binding post connectors are included in the kit.



For cosmetic purposes when the speakers are intended for domestic hi-fi reproduction, grille frames and fabric are supplied, but the response is optimized for monitoring without grilles in place.

The kit includes all components incl. flatpack cabinets machined from 18 mm MDF. The cost of the kit is £329 per pair incl. VAT plus £15 carriage. Write for full specification to **Wilmslow Audio Ltd • Wellington Close • Parkgate Trading Estate • KNUTSFORD WA16 8DX • Telephone (0565) 50605.**

BESofT ELECTRODRAW

BESofT ELECTRODRAW for the Sinclair ZX Spectrum is a versatile program for drawing, editing, storing and printing electrical circuit diagrams.

It is very easy to use, mainly by number keys, cursor keys and initial letter of function.

The 50 symbols supplied include all the most frequently used electronics and logic gate symbols.

Memory space allows up to 400 more user-defined symbols, enabling ELECTRODRAW to be readily adapted for other drawing disiplines such as architectural diagrams and process plant schematics.

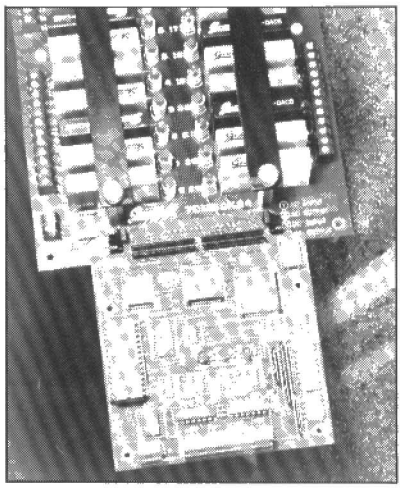
Symbols and labels may be rotated and 'flipped' to give any required orientation.

Symbols and labels can be 'dragged' into exactly the required position on the diagram.

There are many more features: for details of these, contact **BESofT • 20 Ashville Road • LONDON E11 4DT • Telephone (evenings only) 01 558 3469.**

CONTROLLER CARD FOR EASY PC PROGRAMMING

Available from Highland Distribution is the Grayhill ProMux industrial controller card: an EEPROM-based unit designed to interface with the company's range of industrial I/O modules (also available from Highland).



ProMux is designed specifically to be easy to program directly from an IBM or compatible PC and stores preprogrammed commands for actuation every time the system is powered up.

Highland Electronics (Distribution) Ltd Albert Drive • BURGESS HILL • RH15 9TN • Phone (0444) 66000.

TRAVELLING-WAVE TUBES

B. Higgins

Although many electronics engineers are not familiar with their basic operation and applications, travelling-wave tubes (TWTs) are important components used in satellites and other microwave applications. Their use has increased rapidly in line with the widening of the available radio spectrum and the continuing development of satellite communications systems. Recently commissioned medium and high-power TV satellites such as Astra 1A, DFS Kopernikus, TV-SAT2, TDF-1 all use high-performance TWTs to provide television pictures around the clock to millions of viewers.

A travelling-wave tube is an electronic amplifier for microwave radio signals. It is not, strictly speaking, a thermionic tube, but rather a complete wideband RF power amplifier in a vacuum envelope. Originally developed in the mid 1940s, TWTs have been improved considerably since then. In particular, their power efficiency has gone up over the years from a modest 10 to 20% to nearly 50% for the latest types used in direct-broadcasting TV satellites.

The radio signals produced by TWTs are normally in the frequency range from 2 GHz to 22 GHz, spanning the S, C, X, Ku and Ka bands. Table 1 lists the 10 different TWTs operating at frequencies spread across these radio bands.

The outstanding feature of the TWT is its high power gain of 30 dB to 55 dB. This means that an input power of less than 1 mW is sufficient to achieve an output power of tens of watts across a wide frequency range. Disadvantages of the TWT are its size and weight, relatively low efficiency, and high-voltage power supply requirement.

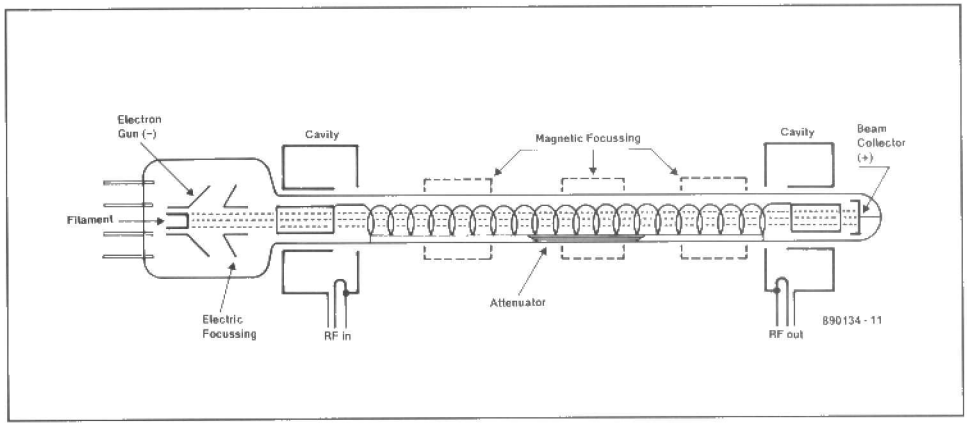


Fig. 1. Basic helix travelling-wave tube (TWT) with magnetic focussing.

How it works

The principle of operation is illustrated in Fig. 1. The electron beam produced by a filament, cathode and associated gun structure travels along the axis of the TWT, before being collected by one or more electrodes (collectors). The helical circuit spaced closely around the beam axis has a structure that causes it to propagate an RF wave that is slow with respect to the speed of light. The helix propagation velocity depends on the power rating of the TWT, and is typically 10–30% of the speed of light. An input cavity is provided to couple the RF signal to the 'slow' wave structure. The amplified RF output signal is similarly taken from a cavity.

The collector voltage and filament emission are accurately controlled so that the velocity of the electron stream is approximately the same as the axial phase velocity of the RF input wave on the circuit. If the helix is properly proportioned, its phase velocity is almost independent of frequency over a wide range. It is, therefore, not uncommon for a TWT to have a bandwidth of more than an octave.

The electron stream is density-modulated because the longitudinal component of the field generated by the 'slow' wave interacts with the electrons travelling in approximate synchronism with it. The result of the modulation is that the electron stream induces additional waves on the helix. Thus, along the length of the tube, a portion of the direct-current energy of the

Frequency Range (GHz)	Output power (W)	Mass (kg)	Type number	Manufacturer	Radio band
2.5 to 8	500	4.5	500CW	Teledyne	S
3.5 to 12	30	0.68	QKW5004	Raytheon	S
3.7 to 4.2	10	0.68	TL4010	AEG	S
4.5 to 10	1.5	0.9	N1078	EEV	C
7.9 to 8.4	60	–	N10025	EEV	C
6 to 18	40	0.68	QKW5005	Raytheon	X
8 to 18	2	0.7	N10024	EEV	X
12 to 12.8	20	0.7	TL12019	AEG	Ku
14 to 14.5	200	3.2	Ku200W	Teledyne	Ku
29 to 31	12	1	TL30011	AEG	Ka

Table 1. Across the spectrum spread: listing of ten TWTs capable of working at different bands in the radio frequency spectrum.

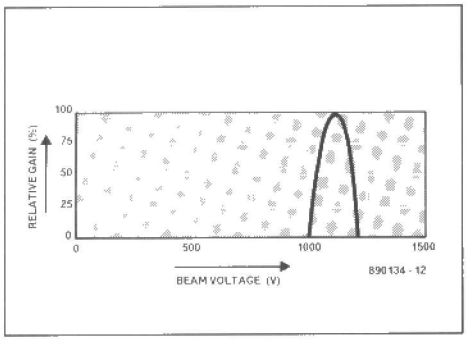


Fig. 2. Typical relative TWT power gain as a function of accellerating voltage.

electron stream is transferred to the circuit as RF energy, resulting in amplification of the RF input wave.

The all-important synchronism between the electron beam and the RF requires accurate control of the accelerating voltage, which is by no means simple to implement in a spacecraft. The graph in Fig. 2 shows the typical dependency of the RF power gain on the beam accelerating voltage.

Magnetic focusing

In order to control the physical size of the electron beam in a TWT a focusing field is required, providing a strength that enables the charge forces to be compensated that would otherwise cause excessive beam divergence. The need of weight and size reductions in satellites have forced the development of permanent-magnet focussing structures in which the field is reversing periodically. Owing to various technical limitations, electrostatic focusing has not (yet) proved a viable alternative to magnetic focusing.

A carbon-based attenuator structure is often fitted along the beam axis to enhance the stability of the TWT (at gains of more than 50 dB, oscillation is a real hazard).

THEORETICAL BACKGROUND TO TRAVELLING-WAVE TUBES

The electron velocity, v, in cm/s is a function of the accelerating voltage, V, as expressed in

$$v = 5.93 \times 10^7 V^{1/2}$$

The approximate power gain, G, in decibels, of a TWT may be calculated from

$$G = A + BCN$$

where
A is the initial mode establishing loss on the helix. Typical values are 6 dB to –9 dB;
B is a gain coefficient representing circuit attenuation and space charge;
C is a gain parameter determined by the impedances of the circuit and the electron stream;
N = the number of active wavelengths in the tube.
Factor C is accounted for by

$$C = \sqrt[3]{\frac{E^2}{(\omega/v)^2} P \times \left(\frac{I_0}{8 V_0}\right)}$$

and N by

$$N = (l/\lambda_0)(c/v)$$

where
I_0 = beam current
V_0 = beam voltage
l = axial length of the helix
λ_0 = free-space wavelength
v = phase velocity of wave along tube
c = speed of light.

Voltages and currents

To obtain maximum efficiency from a TWT, its operating voltages are all-important. There are 3 main voltages to consider: the collector voltages, the helix voltage, and the heater voltage. Table 2 list the voltage and current specifications of a number of TWTs.

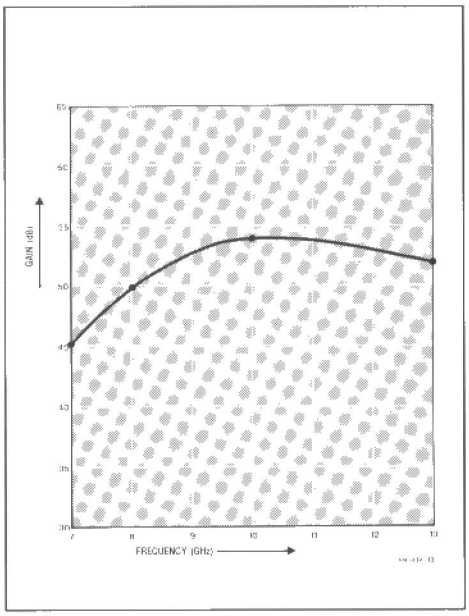


Fig. 3. Typical TWT small-signal gain characteristics.

Collector voltages are usually of the order of 2 kV, although the current trend is towards voltages below 1 kV. Collector current is typically between 20 mA and 1 A. Voltage regulation to within 10% is required for reasons outlined above. Multiple collectors can help to increase efficiency.

Helix voltages are typically between 2 kV and 10 kV, and currents between 10 mA and 500 mA.

The heater voltage, finally, is between 3.5 V and 6.3 V at a current demand of 0.5 A to 2.5 A. The filament heats up the cathode to a temperature of about 650 °C to enable electron emission to take place.

Type	Voltage (kV)				Current (mA)					
	Collector 1	Collector 2	Helix	Heater (V)	Cathode	Collector	Helix	Heater (A)	Efficiency (%)	Gain (dB)
500CW	4.2	2.2		6.3	650		65	3.4		
QKW5004	1.45		2.5	6.3		135				55
TL4010			1.55		37				40	
N1078	2		2		25					37
N10025	2.1				49				34	28
QKW5005	1.8		3.8	6.3		135	12	0.5		40
N1024	2.5		2.5			22				
TL12019			4.2		44				37	
Ku200W	8.6			6.3	215		3	1.4		
TL30011			5		38				29	

Table 2. Electrical characteristics of a selection of TWTs.

Special applications and developments

Pulsed TWTs have been developed to produce a short coherent burst of RF energy, for radar applications. The frequency, bandwidth and peak-power specifications of these special TWTs have been optimized to meet the demands of radar users.

Modern metallurgical processes have enabled TWTs to be produced with a low mass and special alloy focusing magnets that give accurate beam control. Low mass of the TWT and, of course, its associated multi-voltage power supply, are prime considerations to keep the payload weight of launch vehicles to a minimum.

What to look forward to

Recent history has seen industry commitment for delivery of amplifiers that cover the frequency range of 10.7 GHz to 12.7 GHz, mainly as a result of the increasing use of satellite-TV in the communications and direct-broadcasting segments of the X and Ku radio bands. Tube designs that can address this whole bandwidth are in the inventory of a number of major TWT manufacturers including Telefunken, Varian Associates, T-CSF and Hughes EDD. It is important, however, to recognize that new circuit technologies based on 2-stage collectors are showing promise of efficiencies previously associated only with 4-stage collector designs. In addition, these 2-stage collector designs are expected to yield substantially improved phase linearity over 'classic' designs and could, to a large extent, help to remove, or at least relax the requirements of, linearization devices from future TWT systems.

Research has shown that a typical Ku-band satellite-TV TWT with a bandwidth of 2 GHz and a 2-stage collector may be expected to exhibit greater than 50% efficiency with a 4-stage depressed collector. The previously mentioned developments in TWT technology, however, allow devices to be produced that provide efficiencies up to 54% with 2-stage collectors. In these new TWTs, the 2-stage collector has not been modified. The circuit improvement, which primarily involves optimization of velocity taper techniques, produces beam efficiencies of the order of 27–30%, which is significant at X and Ku-band frequencies. In addition, these new circuits further reduce phase distortion with typical AM-PM conversion at 2 to 4 dB. Also, third-order intermodulation (IM) products are significantly reduced. At saturation, the two-carrier third-order IM product is not less than 14 dB down from single-carrier saturation.

In conclusion, it is interesting to project the performance, and in particular the efficiency, of TWTs that utilize these new techniques with 3 or 4-stage collectors. Conservative estimates would place minimum TWT efficiency at 58 to 60% for the next generation of low-mass devices.

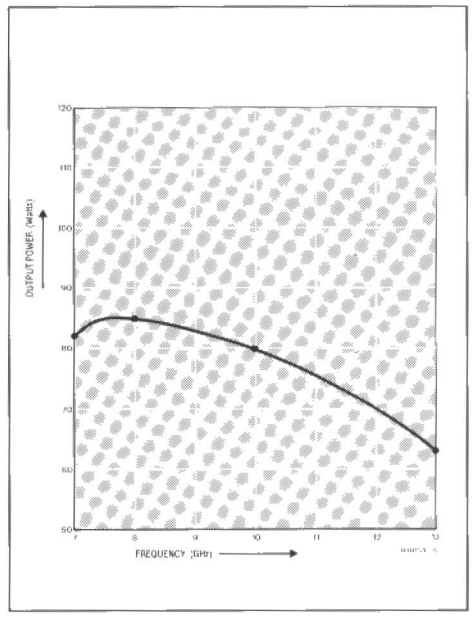


Fig. 4. Typical TWT saturated power output as a function of RF input frequency.

NEW PRODUCTS

Solid-state disk drive

The new SSDD (solid-state disk drive) from DSS Innovative Electronics bv of the Netherlands takes the place of magnetic storage devices such as floppy and hard disk drives in IBM PC/XT/AT and compatible computer systems.

The absence of moving parts on the SSDD increases both the speed and the reliability of personal computer systems. The DOS operating program can be stored on the SSDD, just like other programs to improve the computer's ability to withstand vibration, dust, dirt etc.

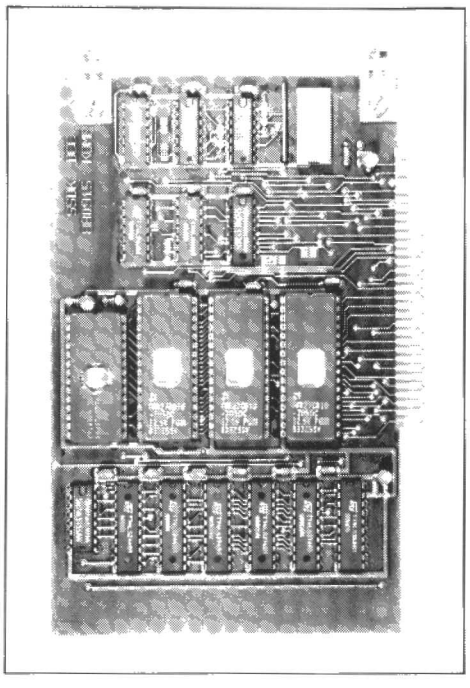
The SSDD emulates a floppy disk or hard-disk drive by means of a unique BIOS routine. Modifications to the IBM BIOS on the personal computer are not necessary. The SSDD can operate in two different modes:

Autoboot:

The SSDD replaces floppy drive A. The computer starts up from the SSDD.

File mode:

Programs and files are stored on the SSDD. In this mode, normal installation of DOS on a disk drive is necessary.



The SSDD is available in versions with a capacity from 256 KBytes to 1 Mbytes.

The AUTHORIZER software security package is an option for the SSDD. It dynamically generates more than 16 million codes that can be embedded in a program. The total number of unique AUTHORIZER security combinations that can be produced amounts to 100 billion. This makes copying programs safeguarded by AUTHORIZER pointless as such programs can no longer be executed.

Applications of the SSDD include diskless personal computer systems, industrial controllers, very fast control systems, standalone and turnkey measuring systems, and PC workstations in a network environment. The latter application is currently of particular interest because it prevents unauthorized persons copying or manipulating confidential files from a central computer. Also, since there is no floppy disk drive, it becomes much harder to introduce a virus into the system.

Comprehensive software is supplied with the SSDD to enable users to move programs and operating systems from floppy disk to the EPROMs on the plug-in card.

For further information on the SSDD contact

DSS Innovative Electronics b.v. • Accustraat 25 • 3903 LX Veenendaal • Holland. Telephone: +31 8385 41301. Fax: +31 8385 26751. Telex: 12969 neabbs nl.

READERS SERVICES

All orders, except for subscriptions and past issues, must be sent BY POST to our London office using the appropriate form opposite. Please note that we can not deal with PERSONAL CALLERS, as no stock is carried at the editorial offices.
All prices shown are net and customers in the UK should add VAT where shown. ALL customers must add postage and packing charges for orders up to £15.00 as follows: UK, £1.00; Europe, £1.50; other countries, £2.00 (surface mail) or £3.00 (airmail). For orders over £15.00, but not exceeding £50.00, these p&p charges should be doubled. For orders over £50.00 in value, p&p charges will be advised.

SUBSCRIPTIONS

Subscriptions can be provided anywhere in the world: apply to **Elektor Electronics • Worldwide Subscription Service Ltd • Unit 4 • Gibbs Reed Farm • TICEHURST TN5 7HE • England.**

LETTERS

Letters of a general nature, or expressing an opinion, or concerning a matter of common interest in the field of electronics, should be addressed to The Editor. Their publication in *Elektor Electronics* is at the discretion of the Editor.

PAST ISSUES

A limited number of past issues (from July/August 1987 onwards) is available from Worldwide Subscription Service Ltd • Unit 4 • Gibbs Reed Farm • TICEHURST TN5 7HE • England, to whom orders should be sent. Prices including postage for single copies are £1.90 (UK and Europe) £2.25 (outside Europe – surface mail) or £3.75 (outside Europe – airmail).

PAST ARTICLES

Photo copies of articles from January 1978 onwards can be provided, postage paid, at £1.50 (UK and Europe), £2.00 (outside Europe – surface mail), or £2.50 (outside Europe – airmail). These copies may be ordered from our editorial offices in London.

TECHNICAL QUERIES

Although we are always prepared to assist readers in solving difficulties they may experience with projects that have appeared in *Elektor Electronics* during the PAST THREE YEARS ONLY, we regret that these can not in any circumstances be dealt with by telephone.

COMPONENTS

Components for projects appearing in *Elektor Electronics* are usually available from appropriate advertisers in this magazine. If difficulties in the supply of components are envisaged, a source will normally be advised in the article.

BOOKS

The following books are currently available: these may be ordered from certain electronics retailers or bookshops, or direct from our London office.

301 Circuits	£6.25
302 Circuits	£6.25
303 Circuits	£7.95
Data Sheet Book 2	£8.25
Microprocessor Data book	£8.95

BINDERS

Elektor Electronics binder £2.95

FRONT PANELS

	No.	Price (£)	VAT (£)
Intelligent time standard	86124-F	15.70	2.36
Autoranging DMM	87099-F	2.80	0.42
Frequency meter	87286-F	10.75	1.61
Microcontroller-driven power supply	880016-F	28.75	4.31
Preamplifier for purists	880132-F	8.25	1.24
Autonomous I/O controller	880184-F	8.50	1.28
Analogue Multimeter	880035-F	7.00	1.05

ORDER FORM

VAT No. 454 135 463

This order should be sent to:

ELEKTOR ELECTRONICS
(PUBLISHING)
DOWN HOUSE
BROOMHILL ROAD
LONDON SW18 4JQ
ENGLAND

Name	
Address	
	Post code
Telephone	Date

Please supply the following. For PCBs, front panels, EPROMs, and cassettes, state the part no. and description; for books, state the full title; for photocopies of articles, state full name of article and month and year of publication. Please use block capitals. For TERMS OF BUSINESS see overleaf.

Qty	No	Description	Price (£)	VAT (£)	Total (£)

Sub-total (£)	
P&P (£)	
Total paid (£)	

Method of payment (tick as appropriate):
- ☐ Bank draft
- ☐ Cheque (payable to ELEKTOR ELECTRONICS)
- ☐ Giro transfer (our A/c no. 34 152 3801)
- ☐ Postal/money order
- ☐ Access A/c

Card expiry date: Signature:

SOFTWARE

Software in (E)PROMs	No.	Price (£)	VAT (£)
µP-controlled frequency meter 1 × 2732	531	9.00	1.35
X-Y plotter 1 × 2732	532	9.00	1.35
programmable timer 1 × 2732	535	9.00	1.35
GHz pre-scaler 1 × 2732	536N	9.00	1.35
marine computer 1 × 2716	538	7.30	1.10
Jumbo clock 2 × 2716	539	14.60	2.20
Graphics card 2 × 82S123	543	9.60	1.44
printer buffer 1 × 2716	545	7.30	1.10
MSX EPROMmer 1 × 27128	552UK	7.30	1.10
Intelligent time standard 1 × 2764	553	10.00	1.50
Interface for high-resolution LC screens 1 × 2764	560	10.00	1.50
I/O extension for IBM 1 × PAL16L8	561	8.75	1.32
Centronics interface for slide fader 1 × PAL16R4	562	8.75	1.32
µP-controlled radio synthesizer 1 × 27C64	564	10.00	1.50
Portable MIDI keyboard 1 × 2764	567	10.00	1.50
Pitch control for CD players 1 × 2764	568	10.00	1.50
MIDI control unit 1 × 27C64	570	10.00	1.50
The digital model railway (1 × 2764)	572	10.00	1.50
Slave indication unit for I.T.S. 1 × 8748H	700	15.00	2.25
EPROM emulator 1 × 8748H	701	15.00	2.25
Microcontroller-driven power supply 1 × 8751	702	47.50	7.13
Autonomous I/O controller 1 × 8751	704	47.50	7.13
Transmission & reception of RTTY	XSS-100	8.00	1.20
(Send formatted 3.5 in diskette containing MSXDOS.COM and COMMAND.COM)			
FAX interface for Atari ST	FSS-102	8.00	1.20
for Archimedes	ESS 103	8.00	1.20
(Send formatted 3.5 in. diskette)			
Logic Analyser with Atari ST (incl. diskette)	ESS 111	10.00	1.50
Computer-controlled teletext (incl.diskette)	FSS-113	10.00	1.50

PRINTED CIRCUITS

Readers who wish to make their own PCBs (for private and personal use only) can order the relevant drawings from our editorial offices in London, quoting the relevant PCB number and indicating whether they are required on paper or on film. Prices per drawing, including postage & packing, are £1.50 (paper – surface mail), £2.00 (paper - airmail outside Europe), £5.50 (film – surface mail), or £7.00 (airmail outise Europe).

	No.	Price (£)	VAT (£)
FEBRUARY 1989			
MOSFET power amplifier	87096	12.35	1.85
The digital train	87291-1	4.20	0.63
Touch key organ	886077	10.05	1.16
Car service module	86765	3.60	0.54
	886126	4.10	0.62
VHF receiver	886127	7.45	1.12
Dark-room timer	886100	Not available	
MARCH 1989			
Diesel sound generator	880006	Not available	
VHF/UHF wide-band amplifiers	880186	Not available	
Power line modem	880189	6.10	0.92
ATN Filmnet decoder	890002	Not available	
Centronics buffer	890007-1	19.60	2.94
	890007-2	2.15	0.33
	890007-3	8.35	1.26
APRIL 1989			
The digital train	87291-2/3	4.30	0.65
Class D amplifier	880009	Not available	
DLF frequency reference	880197	Not available	
Function generator	UPBS-1	1.95	0.29
Triplet	890013-1	6.65	1.00
	890013-2	6.80	1.02
Multi-point IR control	890019-1	3.45	0.52
	890019-2	4.05	0.61
Video recording amplifier	889502	See advert on pp.8-9	
MAY 1989			
RDS decoder	880209	Not available	
Digital model train (4)	87291-4	5.25	0.79
Analogue Multimeter	890035	12.50	1.88
In-line RS-232 monitor	890036	Not available	
Code converter for Centronics-compatible printers	890058	Not available	
DTMF system decoder	890060	6.50	0.98
Transistor tester	896029	Not available	
Sine wave converter	UPB-S1	1.95	0.29
Super-VHS to RGB converter	See advert on pp. 8-9		
JUNE 1989			
8-digit frequency meter	880128	11.50	1.73
In-line RS232 monitor	890036	Not available	
In-circuit transistor tester	890079	Not available	
Echo unit	See advert on p.8-9		
July/August 1989			
MIDI keyboard interface decoder board	890105-1	7.00	1.05
controller board	890105-2	5.25	0.79
Tracking tester	See advert on pp. 8-9		
Test pattern generator	890020	Not available	
DC-AC power converter	890056	Not available	
Floppy disk monitor	890078	4.25	0.64
display board	85019	3.25	0.48
Function generator	UPBS-1	1.95	0.29
Call tone generator	894016	Not available	
Sound level meter	894024	3.50	0.53
Mains-failure indicator	894030	Not available	
Radio beacon converter	894041	Not available	
Low-noise microphone preamplifier	894063	3.75	0.56
Bucket brigade delay line	894055	3.75	0.56
SEPTEMBER 1989			
Digital model train	87291-IV	6.70	1.00
Stereo viewer	890044	5.57	0.86
Simple FM receiver	890118	Not available	
Centronics monitor	890123	5.50	0.83
Resonance meter	886071	3.90	0.59
OCTOBER 1989			
Inductance meter	890119	7.25	1.09
Logic analyser with Atari ST	890126	5.25	0.79
CD error detector	890131	6.00	0.90
16-channel running lights	896072	Not available	
RGB to CBS converter	See advert on pp. 8-9		
NOVEMBER 1989			
Digital model train (8)	87291-5	43.50	6.53
Extension Card for Archimedes	890108	18.00	2.70
Extension card for Archimedes incl. PAL/floppy	890108-9	29.25	4.39
3½ LED-digit SMD voltmeter	890117	3.75	0.56

ORDER YOUR COPY OF THE NEW MAPLIN CATALOGUE ON SALE SOON

Pick up a copy from any W.H. Smith for just £2.25 or post this coupon now to receive your copy for just £2.25 + 50p p & p. If you live outside the U.K. send £4 or 17 International Reply Coupons. I enclose £2.75.

Name .....

Address .....

.....

Post Code .....

Send to Maplin Electronics, P.O. Box 3, Rayleigh, Essex SS6 8LR.

AVAILABLE FROM 10th NOVEMBER 1989 IN ALL W.H. SMITH STORES

E 90

OVER 580 PAGES WITH HUNDREDS OF NEW PRODUCTS AT SUPER LOW PRICES

THE NEW MAPLIN CATALOGUE – WORLDS APART!

1990 BUYER'S GUIDE TO ELECTRONIC COMPONENTS SEND FOR YOUR COPY TODAY